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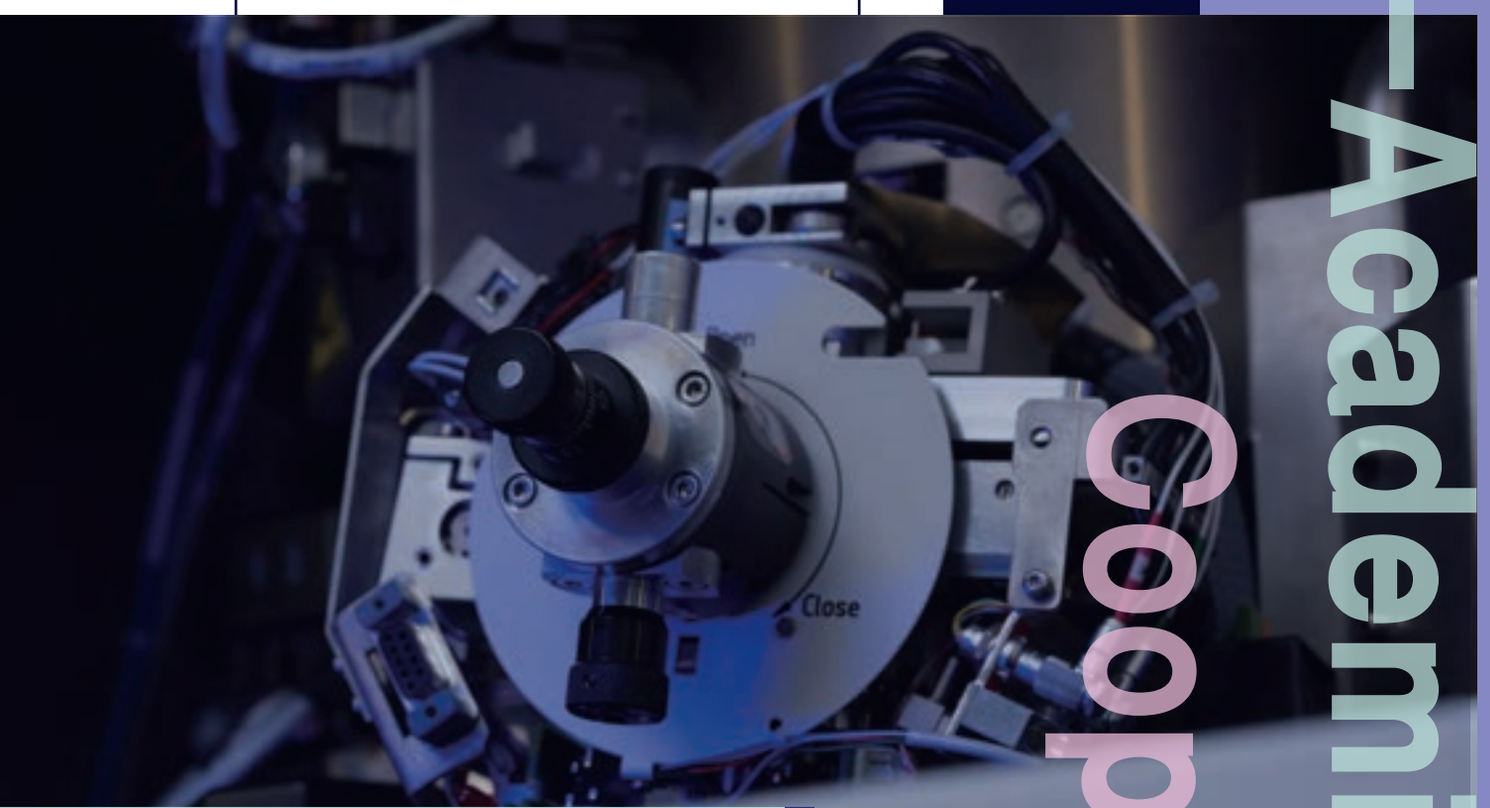

MATERIAL ANALYSIS TECHNOLOGY INC.

閎康科技產學合作計畫

111

年度成果發表

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閎康科技自2021起，攜手科技部，針對多所國立大學，提供每年新台幣2,000萬元的研發經費，希望藉此強化研發能力，促進產業升級。

第二屆111年度產學合作計畫於2022年8月正式展開，公開徵件共徵得投稿計畫書逾五十餘件，涵蓋領域包括先進半導體、光電材料、製造封裝至生醫等領域。

閎康科技是台灣第一家提撥經費攜手學界研發的半導體研發實驗室，在111年度的產學合作計畫眾多徵件投稿中，看到台灣學界實驗室研發的各種潛力與可能性，希望藉由提升研發過程中的分析檢測品質，協助更多優秀的研發計畫得以實現，讓企業與學術單位共獲雙贏。

閎康科技為設備齊全的分析檢測實驗室，擁有高產能、高機台能力以及高水準的分析服務品質。

技術團隊擁有橫跨三大半導體產業的專業知識，包含積體電路(IC)、光電元件(Optoelectronics)、平面顯示器(Flat Panel Displays)等不同產業領域多年的實際品質管理及技術分析經驗。

服務範疇涵蓋電子產品設計階段的快速除錯、實體驗證，以及微奈米產品元件的缺陷精準定位、結構觀察、材料成分等各種動靜態分析；舉凡製程開發、製程整合、基礎學術研究、品質管制、專利訴訟、故障分析、競品分析，或是客戶退貨等各類問題皆在閎康的服務範圍內，提供各領域完整解決方案。

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National Sun Yat-sen University

Chang, Liu-wen

DEVELOPING A NOVEL METHOD TO CHARACTERIZE CRYSTALLINITY OF EPILAYERS GROWN ON POLYCRYSTALLINE SUBSTRATES USING ELECTRON BACKSCATTER DIFFRACTION (EBSD) TECHNIQUE

以電子背向散射繞射技術分析多晶基板上成長的磊晶的結晶性

Liu-wen Chang **張六文**

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National Sun Yat-sen University, Taiwan

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Research Team:

劉士滙/施政宏

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-001.

*The CrossCourt simulation of this study is supported by Prof. Jui-Chao Kuo at National Cheng Kung University

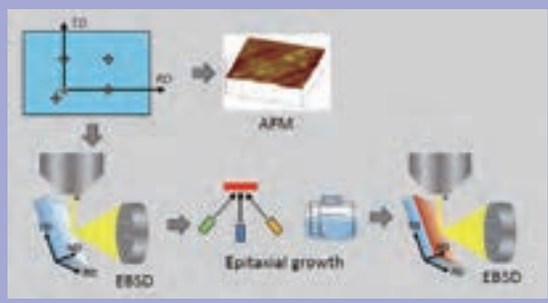
Introduction

High-resolution X-ray diffraction (HR-XRD) and transmission electron microscopy (TEM) techniques have long been used to analyze crystallinity and defects of epilayers grown on single-crystal substrates.

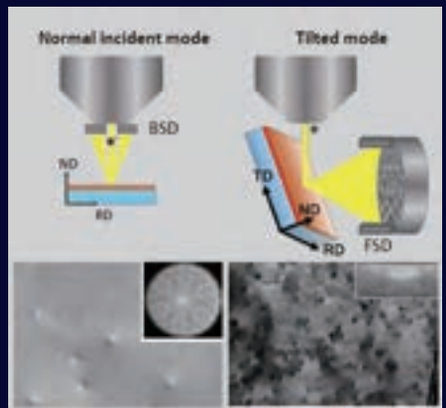
Recently, a combinatorial substrate approach using polycrystalline substrates was proposed for high throughput research of epitaxy. The HR-XRD technique, however, cannot be used to analyze the epilayers on polycrystalline substratesanymore, whereas the TEM technique is time consuming. This study therefore aims at developing alternative techniques based on scanning electron microscopy (SEM). Electron backscatter diffraction (EBSD) is a SEM based technique which provide crystal structure/orientation information of the samples. The angular resolution of EBSD is however not high enough for epitaxial analysis.

Recently, a couple of methods using post-treatment to improve the angular resolution have been proposed. Moreover, the channeling imaging technology can further provide the information of the grown-in defects.

Accordingly, the integration of techniques mentioned above can provide an effective way for the characterization of epilayers.

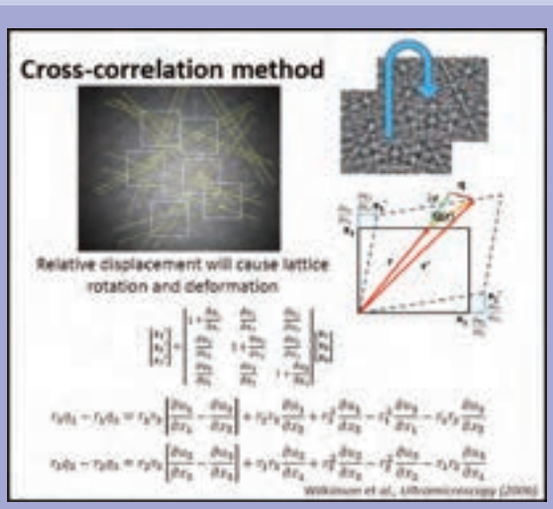


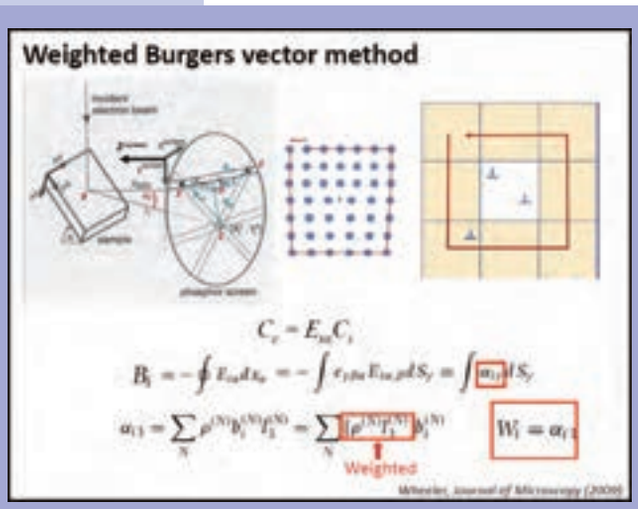
COMBINATORIAL SUBSTRATE APPROACH FOR EPITAXY



ELECTRON CHANNELING PATTERN (ECP) & ELECTRON CHANNELING CONTRAST IMAGING (ECCI)

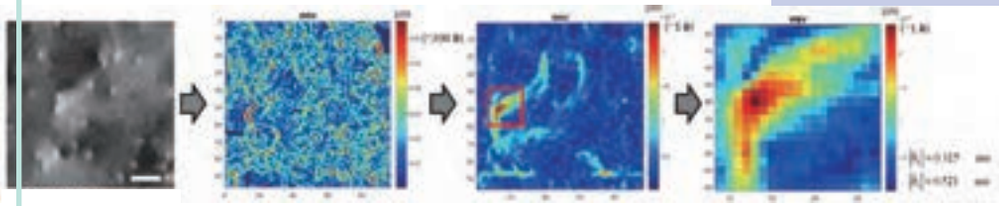
MATERIALS & METHODS



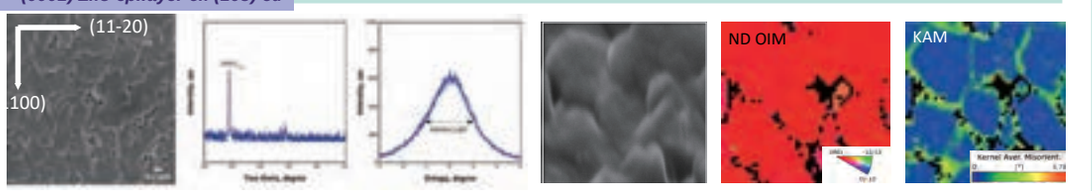


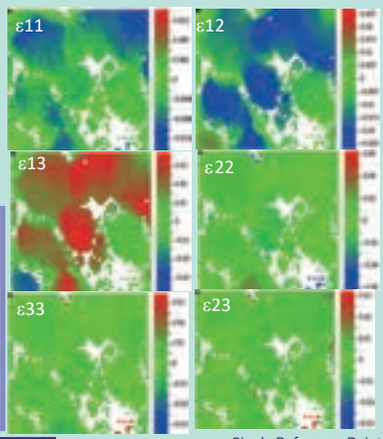
RESULTS & DISCUSSION

ECCI: (0001) GaN epilayer



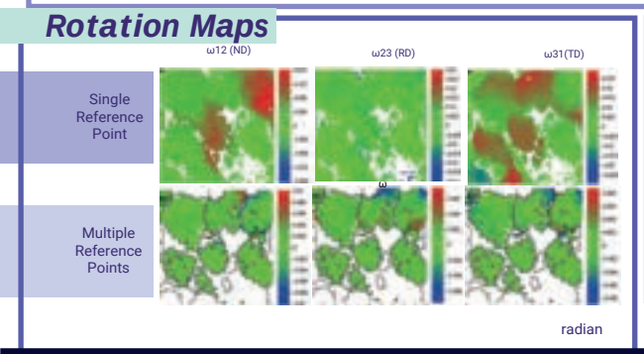
(0001) ZnO epilayer on (103) Cu

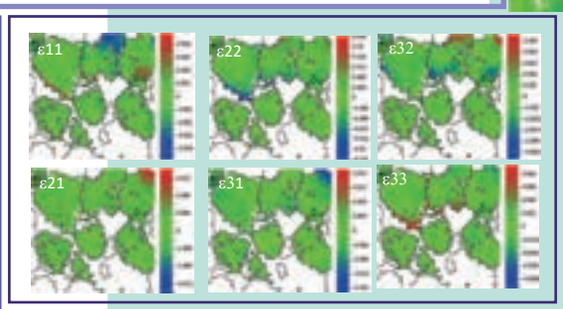




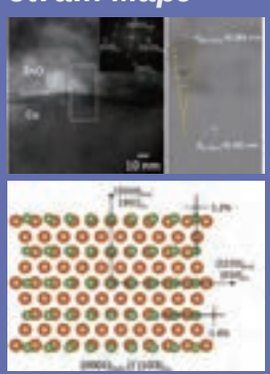
Single Reference Point

Rotation Maps





Strain Maps

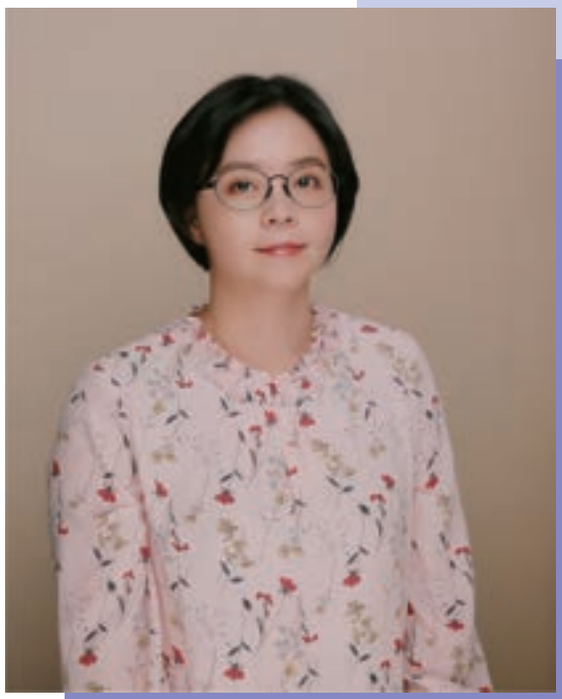


Conclusion

This study has developed technique for acquiring ECP and ECCI in SEM. The density of threading dislocations in a GaN epilayer was estimated directly from the ECCI. The strain field around the dislocations was also quantified using the weight Burgers vector method based on orientation data collected from EBSD. In addition, a (0001) ZnO epilayer grown on (103) Cu substrate was analyzed by EBSD. The EBSD data was post-treated by the CrossCourt software and the relative rotation and elastic strain were calculated accordingly. The growth behavior of the ZnO crystals can be well-explained by the rotation/strain data derived. The present results demonstrate that the SEM-based techniques can be a good alternative for epilayer analysis.

National Central University

Hsu, Yi-chiung



ENGINEERED BIOMIMETIC TISSUES FOR EVALUATION OF CANCER DRUG TREATMENT MODELS

工程仿生組織建構用於癌症藥物治療模型評估

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-002.

*The confocal experiments and image data analysis of this study were conducted in collaboration with Dr. Ming-You Shie.

Introduction

Cancer remains a significant global health challenge, necessitating the development of effective drug therapies. However, the evaluation of anticancer drugs requires accurate and reliable models. To address this, we employ engineering biomimetic tissues as a platform for assessing the efficacy and toxicity of cancer drug treatments.

The construction of biomimetic tissues involves embedding cancer cells within a three-dimensional scaffold that mimics the physiological characteristics of natural tissues, thus creating a crucial environment for tumor development, including cell proliferation, invasion, and response to treatment.

To assess the effectiveness of cancer drug therapies, we combine genetic analysis techniques to provide mechanistic insights into drug responses, serving as a preclinical model for evaluating cancer drug treatments.

With this innovative approach, we hope to advance our understanding of cancer treatment efficacy, paving the way for developing more targeted and efficient therapies to combat this global health challenge.

Conclusion

The study utilized cell-derived spheroids on a model to investigate the toxicity of chemotherapy drugs. The comparison was made between 2D and 3D models to evaluate their respective responses to the treatment. Our results revealed that the 3D model exhibited higher resistance to the chemotherapy drugs than the 2D model.

In our study, we observed that the 3D cell-derived spheroids displayed increased resistance to the chemotherapy drugs, doxorubicin, and taxol, as compared to the 2D monolayer cultures. This finding aligns with previous research highlighting the enhanced drug resistance exhibited by cells in 3D models. The 3D spheroids may provide protective niches for tumor cells, leading to reduced drug accessibility and impaired drug efficacy.

RESULTS

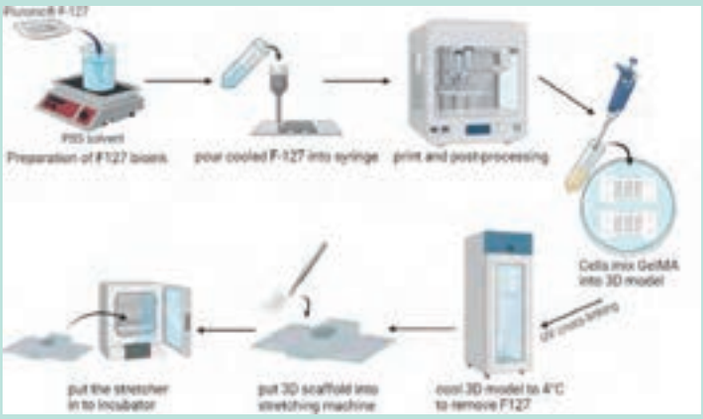

FIGURE1. SCHEMATIC OF THE FABRICATION PROCESS AND USE OF THE DEVELOPED TUMOR SPHEROID MODELTO PREDICT THE OPTIMAL CHEMOTHERAPY DRUG.

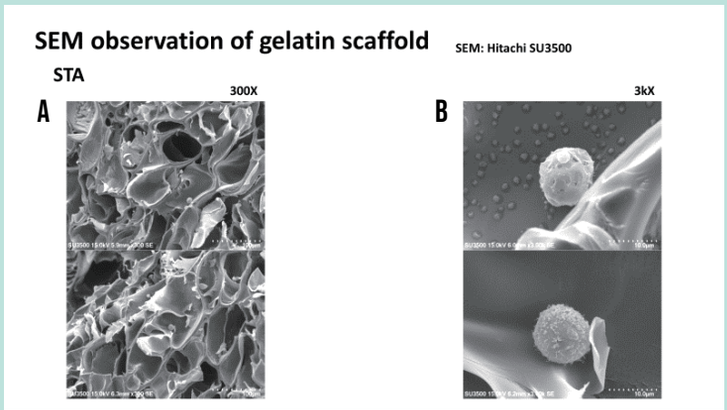

FIGURE 2. CHARACTERIZATION OF 3D SCAFFOLDS. (A) SEM IMAGES OF 3D SCAFFOLDS & (B) 3D CULTURED CELLS.

FIGURE 4. CANONICAL PATHWAYS DERIVED FROM GENES IN THE LEADING EDGE, ANALYZED USING IPA PATHWAYS.

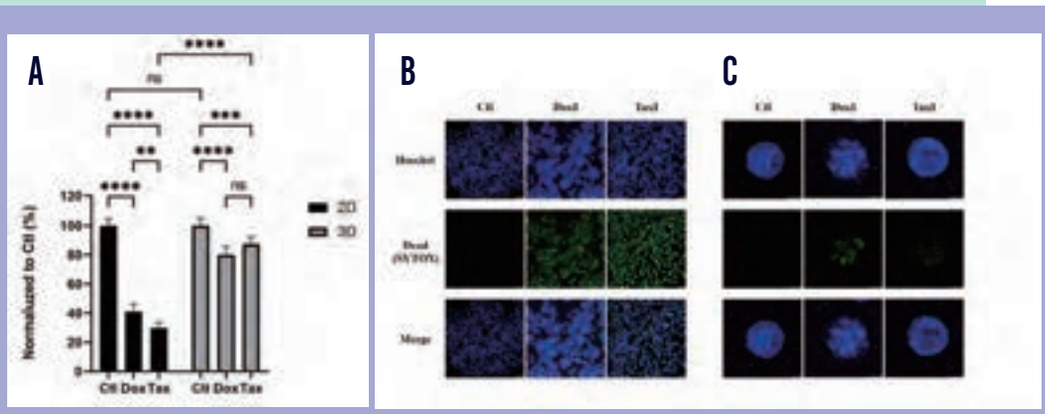

FIGURE 3. CELL-DERIVED SPHEROIDS ON A MODEL ARE USED TO ASSESS THE TOXICITY OF CHEMOTHERAPY DRUGS. THE MODEL IS TREATED WITH DOXORUBICIN, AND TAXOLFOR 2 DAYS. (ACELLVIABILITY IS DETERMINED USING THE PRESTOBLUE® REAGENT.CELL MODEL STAINING WITH LIVE/DEAD KIT IN(B) 2D AND (C) 3D CELL MODELS.

MATERIALS & METHODS

3D Spheroids Model

All cells were cultured in their respective appropriate medium. After gelation, the culture medium with endothelial cells was added to the wells by the third cartridge. Each culture medium was changed every 2 or 3 days.

Scanning electron microscopy

Observing samples of 3D scaffolds using a Scanning Electron Microscope (SEM) such as the Hitachi SU3500 can provide valuable insights into the structure, and morphology (MA-tek).

Live/dead analysis

Assessment of the survival and growth of HC in hydrogels using a Live/Dead Kit following the manufacturer's instructions.

RNA-Seq Data Analysis

Total RNA was extracted from clinical tissue samples, tissue-derived cells, and tissue-derived spheroid using a NucleoSpinRNA Kit.

Functional Enrichment Analysis

Canonical pathways analysis found by core analysis in IPA are given with a p-value.

Discussion

Our study provides valuable insights into the differential responses of 2D and 3D models to chemotherapy drugs, as well as the association between RNAseq-based gene expression profiles and drug sensitivity in tumor cells. The utilization of 3D cell models and RNAeq analysis opens up new avenues for research and drug development in the context of cancer treatment. Further exploration of the identified gene signatures and pathways may pave the way for personalized therapeutic approaches to overcome drug resistance and improve clinical outcomes for cancer patients.

National Cheng Kung University

Lai, Wei-chih

THE DEVELOPMENT OF DOUBLE DIELECTRIC UV GaN-BASED VCSEL

全介質式紫外光GaN VCSEL之研製

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Research Team:

Wen-huei Chu

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-003.

Abstract

This project consists of two parts. The first part is to use the simulation software (COMSOL) to investigate the optical reflectivity of distributed Bragg reflectors (distributed brag reflectors, DBRs) composed of different dielectric combinations. The second part is to fabricate optically pumped vertical-cavity surface-emitting lasers (vertical-cavity surface-emitting lasers, VCSELs) with double dielectric DBRs from the ultraviolet (UVA) laser structure grown on the gallium nitride substrate, and measure its optical properties.

In the first part of DBRs simulation using COMSOL software, the substrate surface is defaulted as the discontinuity boundary condition of the material, and multiple layers of repeated and alternating thin films are added on the substrate as the structure of DBRs for analysis. The simulation results show that under the condition of fewer pairs of DBRs (5 layers), using aluminum oxide (sapphire) as the substrate will improve the reflectivity compared to silicon (Si) substrate.

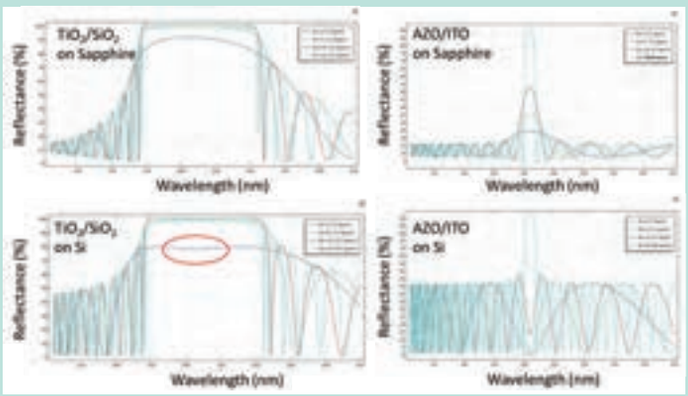
In addition, since the defect density will greatly affect the laser characteristics, the second part of this project will directly use the epitaxy wafers of ultraviolet laser structure grown on the gallium nitride substrate to obtain a high-quality light-emitting layer. The double dielectric DBRs optically pumped UVA VCSEL is fabricated based on the simulation results of the first part.

Conclusion

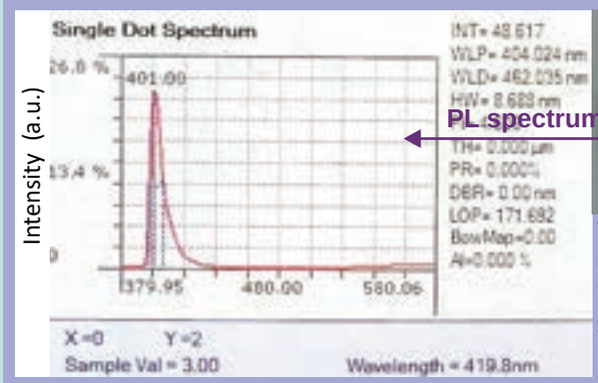
In COMSOL simulation, compared with silicon substrates, sapphire substrates can tolerate fewer pairs to achieve high reflectivity, but the heat dissipation effect is poor. Besides, considering the bandwidth, this research adopts the DBR of TiO_2/SiO_2 structure for experiments. In the beginning, 4 pairs AZO/ITO were sputtered on Si substrate and show about only 30% reflectivity, It may be caused by the incomplete structure as seen in the TEM and EDS image.

RESULTS

COMSOL Simulation



UV GaN-based epitaxy wafer

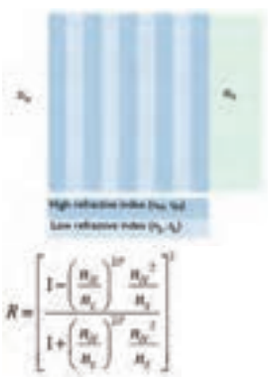


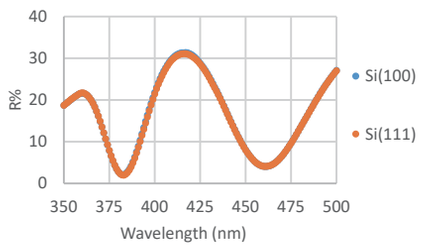
THE CUSTOMIZED GaN-BASED UV EPITAXY WAFER AND THE PL SPECTRUM IN THE CENTER REGION.

DBR

TABLE 1 THE CALCULATION OF REFLECTIVITY OF DBRS.

	Materials	substrate	n_s	n_H	n_L	P	R
p-side	TiO_2/SiO_2	Si	5.3077	2.7366	1.4831	2	0.65847
	TiO_2/SiO_2	Si	5.3077	2.7366	1.4831	4	0.81192
	TiO_2/SiO_2	Si	5.3077	2.7366	1.4831	8	0.90113
	TiO_2/SiO_2	sapphire	1.7849	2.7366	1.4831	2	0.86931
	TiO_2/SiO_2	sapphire	1.7849	2.7366	1.4831	4	0.93239
	AZO/ITO	Si	5.3077	2.098	2.0001	2	0.08527
	AZO/ITO	Si	5.3077	2.098	2.0001	4	0.32476
	AZO/ITO	Si	5.3077	2.098	2.0001	42	0.90087
	AZO/ITO	sapphire	1.7849	2.098	2.0001	2	0.47444
	AZO/ITO	sapphire	1.7849	2.098	2.0001	4	0.69101
	AZO/ITO	sapphire	1.7849	2.098	2.0001	14	0.90003
n-side	TiO_2/SiO_2	Air	1	2.7366	1.4831	1	0.85474
	TiO_2/SiO_2	Air	1	2.7366	1.4831	2	0.92455

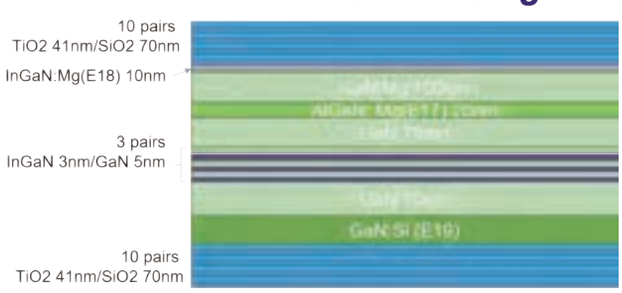




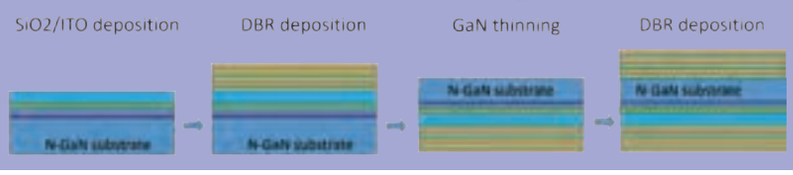
THE REFLECTIVITY OF 4 PAIRS AZO/ITO DBRS SPUTTERED ON SI.

MATERIALS & METHODS

Structure Design



Process Design



Discussion

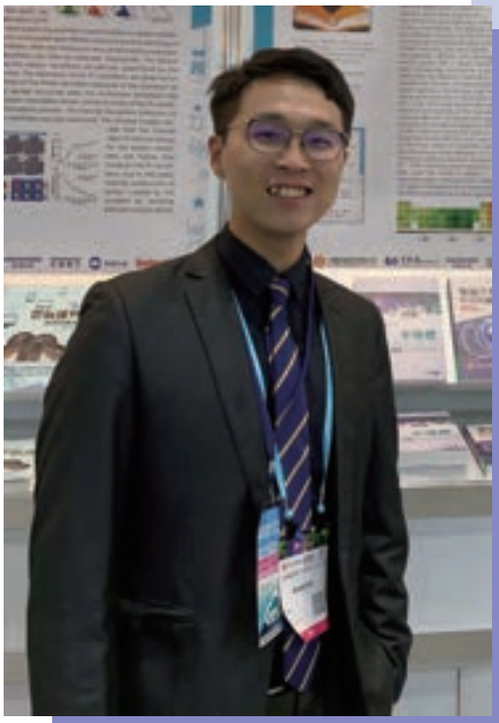
Compared with the silicon substrate, the sapphire substrate can allow fewer pairs to achieve high reflectivity.

It is necessary to achieve a reflectivity above 90%, AZO/ITO DBR requires up to 85 layers of coating. Even if AZO/ITO reaches about 30 pairs, the bandwidth is still smaller than the combination of SiO_2/TiO_2.

4 pairs AZO/ITO were sputtered on Si substrate and show about only 30% reflectivity, It may be caused by the incomplete structure as seen in the TEM and EDS image.

National Cheng Kung University

Liu, Yu-chen



DEVELOPMENT OF NEW LOW-TEMPERATURE SOLDER AND ITS RELIABILITY EVALUATION

新穎低溫銲料開發及其封裝可靠度分析與應用

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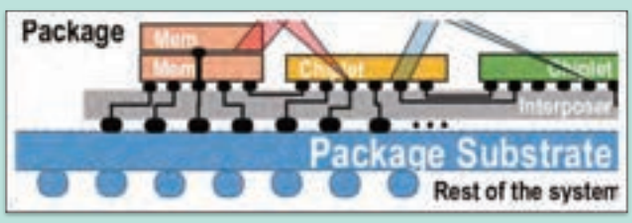
Research Team:

展創

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-004.

Introduction

本計畫的目標為開發高強度、高延展性的低溫銲料系統，並系統性探討所開發之低溫銲料系統之接合可靠度，包含溫度循環測試(Thermal cycling test, TCT)、熱儲存測試(Thermal storage test, TST)、剪切強度(Shear strength)測試，及材料分析。本計畫積極探討Sn-Bi-In合金之高延展性及破斷機制，透過本次產學合作，利用閎康公司提供之高精密分析方法，系統性探討可靠度議題，盼產出高可靠度之低溫銲料系統，並能應用於工業界，以達異質整合封裝之需求，解決翹曲問題(Warpage)。



MING YU LI ET AL., 2008, IEEE TRANSACTIONS ON ADVANCED PACKAGING 31(2):399 - 403

Conclusion

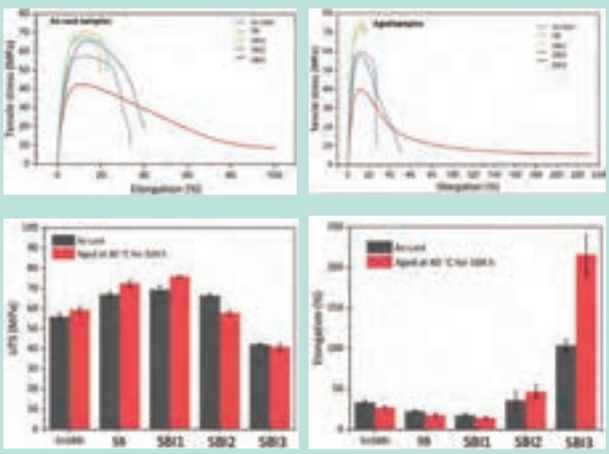
In this study, we proposed the designed Sn-Bi-In alloy with several benefits.

Sn-Bi-In has lower Tm compared to Sn-58Bi, allows lower reflow processing. Additionally, it has smaller contact angle indicates better wettability.

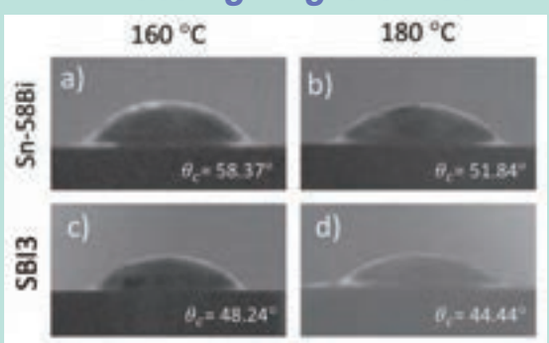
Sn-Bi-In solder has good ductility with adequate strength in as-cast conditions. The performance of solder is even better after thermally aged at 80 0C for 504 h.

RESULTS & DISCUSSION

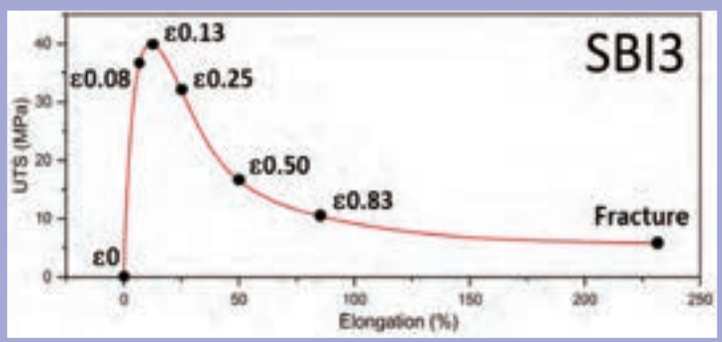
Tensile Property Evaluation



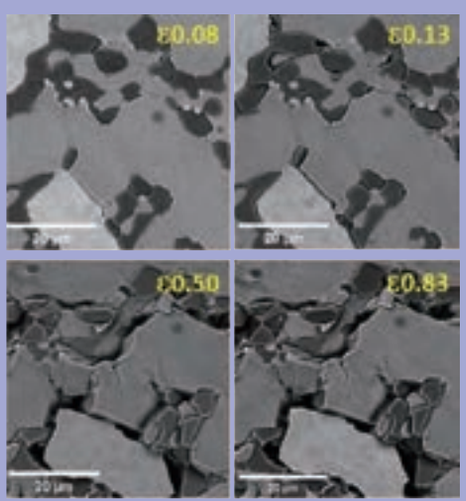
Wetting Angle on Cu



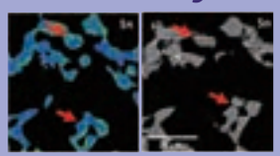
Materials characterization



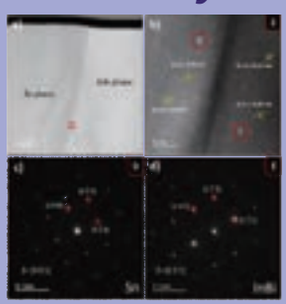
Ex Situ Observation



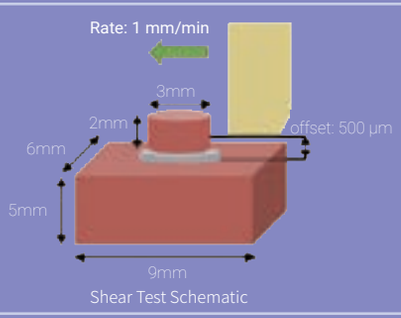
KAM Analysis



TEM Analysis



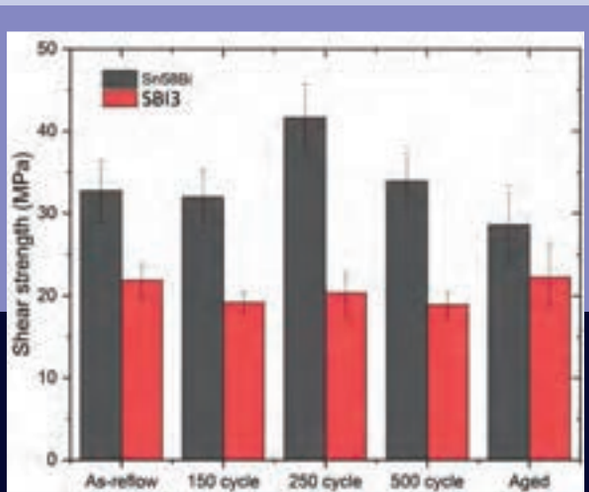
BONDING STRUCTURE EVALUATION

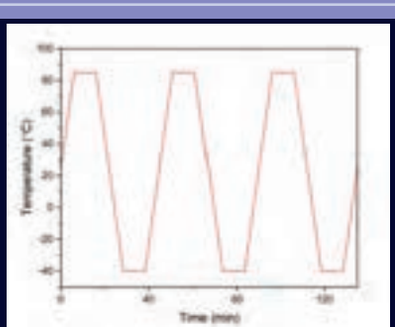


Shear Test Schematic

Thermal aging Parameter:
at 80°C for 504 h

TCT test is confirmed with:
International standard
(JESD22-A104C N condition)





Thermal range : -40 °C to 85 °C
Ramp rate: 10 °C/min
Dwell time: 10 min
Number of cycles:

150 cycles
250 cycles
500 cycles

6 pieces each sample system

National Cheng Kung University

Lee, Wen-shi

LARGE-AREA HIGH QUALITY 2D MATERIAL $MoTe_2$ DEVICE

大面積高品質二維材料碲化鉬元件膜層及電性分析

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-005.

Introduction

電晶體持續往縮小尺寸和堆疊的方向　發展鰭式電晶體以及環繞式閘極結構陸續被提出以提升閘極控制力 、 限制漏電流 如今矽基塊狀材料已縮小至物理 極限面對此挑戰的其中一種策略是使用二維材料。

新興二維材料半導體中最受到廣泛研究的是過渡金屬硫族化合物 (transition metal dichalcogenides TMDs) 以鉬和鎢兩大元素為主搭配 硫族的硫、硒與碲元素組合而成。在厚度二 奈米 以下的奈米片結構 TMDs 可提供比矽基三維塊狀材料更高的載子遷移率以及極低的漏電流。然而　由於　這些超薄材料的垂直維度上只有很少的原子　在使用傳統的製程時很容易在其中引入缺陷和雜質導致性能下降。因此 開發適合二維材料半導體的製程策略至關重要。

本研究開發二維材料半導體製程透過高壓退火 (high pressure annealing) 和鎢元素參雜的方式調控碲化鉬　($MoTe_2$)的相位。藉由及時的尖端材料分析技術微量元素調控的研究得以進行。

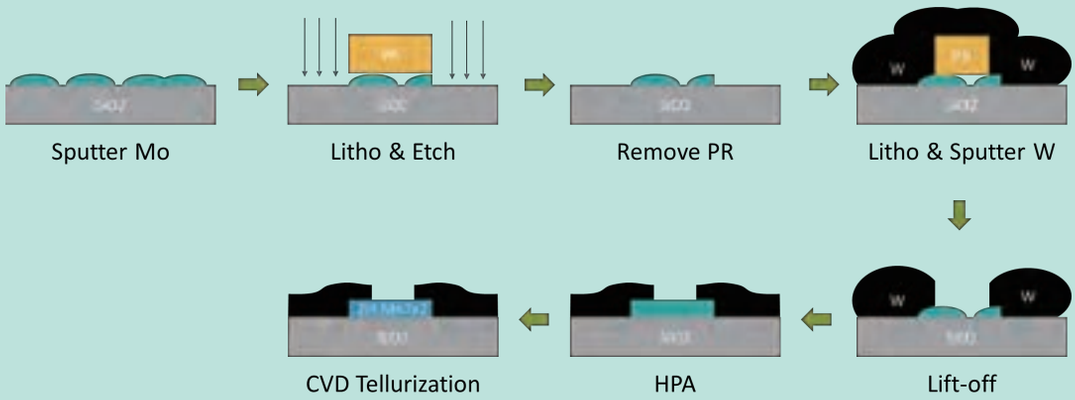
Conclusion

氧氣 HPA 製程可以有效去除鉬膜層中的碳氫雜質。

經過 HPA 製程處理的膜層有較大的製程窗口可形成半導體相位的2H-$MoTe_2$。

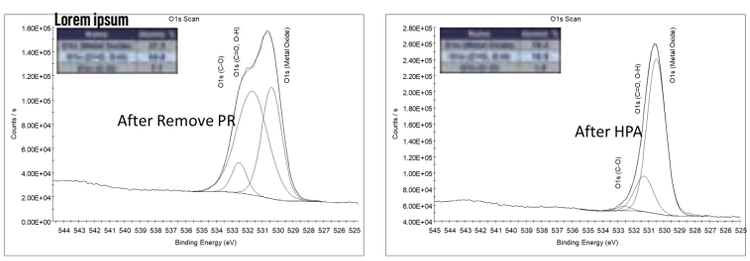
厚的鎢與薄的鉬共同進行高溫碲化可形成一同時含有鉬、鎢和碲的擴散層。

METHODS

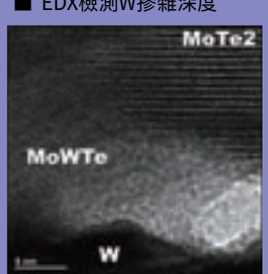


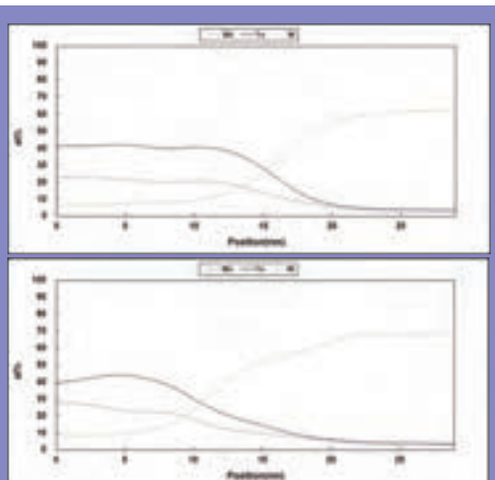
RESULTS

■ XPS檢測HP降低圖案化製程產生的碳汙染

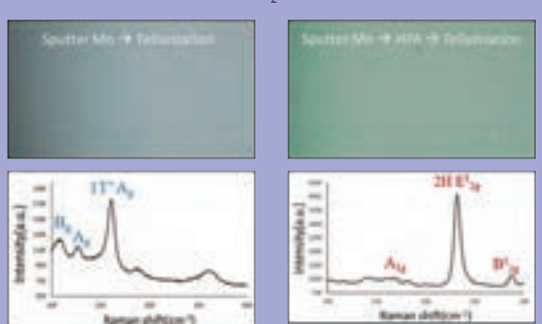


■ EDX檢測W摻雜深度

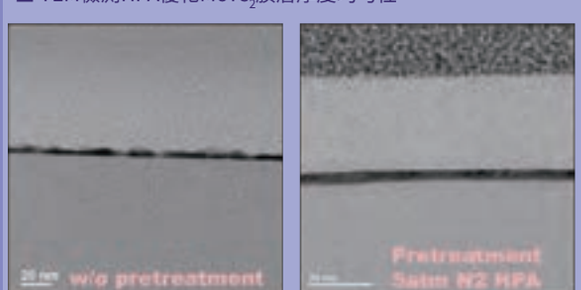




■ Raman檢測HPA控制$MoTe_2$相位、OM性觀察膜層均勻性



■ TEM檢測HPA優化$MoTe_2$膜層厚度均勻性



Discussion

在鉬金屬圖案化後，去除光阻，仍可觀察到碳雜質殘留。透過後續的氧氣HPA製程，碳雜質大幅降低，氧主要與鉬金屬鍵結。

濺鍍鉬後接續CVD碲化，透過TEM可觀察到厚度均勻性不佳，以及1T' 半金屬相位的$MoTe_2$。如果在CVD之前先進行HPA處理，可以觀察到良好的厚度均勻性和2H半導體相位的MoTe2。

在2H-$MoTe_2$製程窗口內，MoWTe層的位置可以透過CVD持溫時間達到約5nm的移動。

National Taiwan Normal University

Lee, Min-hung

NANOSECOND LASER ANNEALING BASED WAKE-UP OF FERROELECTRIC $HfZrO_2$ CAPACITORS FOR BEOL COMPATIBLE AND HIGH THROUGHPUT FERAM

利用奈秒雷射退火開發高產率激活程序且相容於後段製程之鐵電隨機存取記憶體

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-006.

*This study also received supports from National Science and Technology Council (NSTC), Taiwan Semiconductor Research Institute (TSRI), and Nano Facility Center (NFC).

Abstract

Minimizing thermal budget and eliminating wake-up procedure to keep high remnant polarization (Pr) characteristics are the critical issues for ferroelectric RAM (Random access memory).

For former, the Rapid Thermal Anneal (RTA) temperature of ferroelectric $HfZrO_2$ (HZO) crystallization already meets Back End of Line (BEOL) requirement (<400℃). For latter, the mass production is a challenge of wake-up by E-field cycling, which imposes individual device step by step. Recently, several studies on process-based wake-up free are reported such as PEALD (plasma-enhanced ALD), optimized orientation for TiN electrode, NH_3 treatment, etc.

The nanosecond laser annealing (NLA) is proposed for wake-up and made comparison with general E-field cycling on crystallized HZO. This method benefits for improvement the throughput and feasibility, as well as low temperature process to meet the requirement of BEOL. In this project, the insight of the wake-up and fatigue have been studied by MA-TeK supporting.

Conclusion

Nanosecond Laser annealing is proposed to wake up a pristine ferroelectric capacitor and make comparison with conventional E-field cycling.

Nanosecond Laser annealing has advantages of high throughput and low thermal budgets, and is compatible with back-end-of-line (BEOL) process.

The insight of wake-up and fatigue have been studied through STEM HAADF, NBD, GIXRD, and GPA.

The o-phase enhancement of NLA-based FeRAM after NLA is validated.

RESULTS

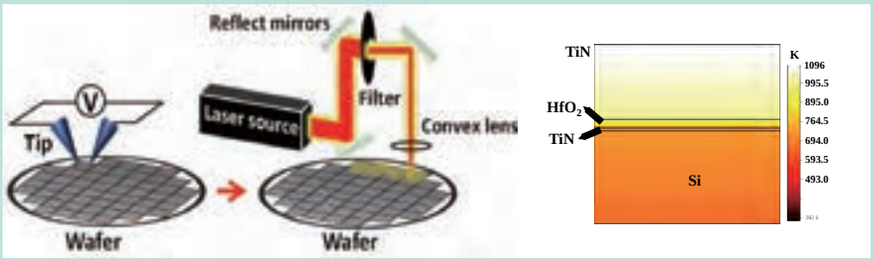

FIGURE1. SCHEMATIC DIAGRAM OF WAKE-UP BY E-FIELD CYCLING AND NANOSECOND LASER ANNEALING (NLA). THE ADVANTAGES OF NLA ARE HIGH THROUGHPUT AND LOW TEMPERATURE FOR BEOL COMPATIBLE.

FIGURE2. CALCULATED TEMPERATURE DISTRIBUTION OF THE MFM CAPACITOR WITH NLA 140 MJ/CM2. THIS INDICATES THE NLA PROCESS APPLICABLE FOR BEOL.

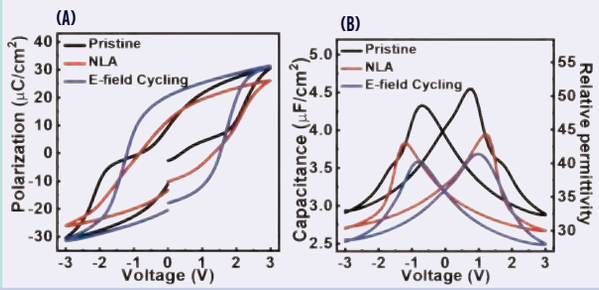

FIGURE3. (A) P-V & (B) C-V CHARACTERISTICS OF PRISTINE, E-FIELD CYCLING, AND NLA. THESE INDICATE THAT BOTH E-FIELD CYCLING AND NLA CAN INDUCE ORTHORHOMBIC PHASE FORMATION.

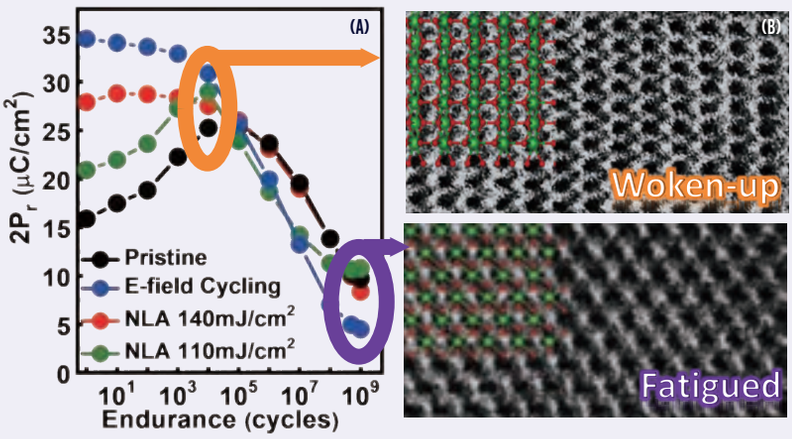

FIGURE 5. (A) THE ENDURANCE CHARACTERISTICS OF PRISTINE, E-FIELD CYCLING, AND NLA. THIS IMPLIES NLA BENEFICIAL FOR WAKE-UP AND AVOIDS OPERATION CYCLING SUCH AS E-FIELD STRESS.
(B) STEM-ABF OF WOKEN-UP AND FATIGUED STAGE. THE UNBALANCED Zr-O BOND LENGTH OF FATIGUED STAGE RESULTS IN ATOMIC STRUCTURAL DISPLACEMENTS IN HZO.

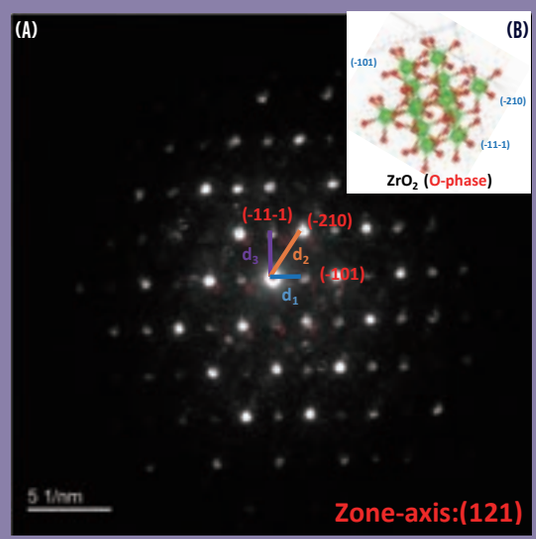

FIGURE 6.

(A) NBD ANALYSIS OF HZO AFTER NLA.

(B) ORTHORHOMBIC PHASE ATOMIC ARRANGEMENT OF Zr BY VESTA. THE ARRANGEMENT OF Zr ATOM AGREES WITH NBD AND VALIDATES O-PHASE AFTER NLA.

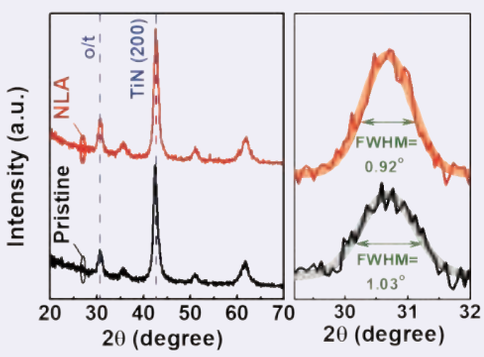

FIGURE 7. GIXRD ANALYSIS OF PRISTINE AND NLA. THIS INDICATES O/T PHASE INCREASING WITH NARROWING FULL WIDTH AT HALF MAXIMUM (FWHM) AT THE PEAK AROUND 30° -31° .

Phase	Color	Phase fraction(%)	
		(a)Pristine	(b)NLA
Orthorhombic		40.4	56.3
Tetragonal		41.4	24.3
Monoclinic		9.3	13.3
Mixed		8.8	4.5

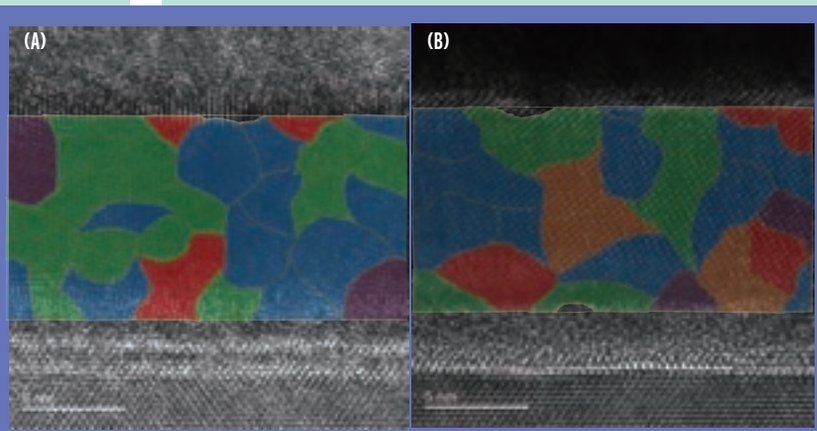

FIGURE 8. GEOMETRIC PHASE ANALYSIS (GPA) OF (A)PRISTINE (B)NLA FROM TEM IMAGE. THE O-PHASE OF NLA INCREASES SIGNIFICANTLY TO VALIDATE THE ENDURANCE RESULTS.

National Tsing Hua University

Chang-Liao, Kuei-shu

PROCESS STUDY OF GATE STACK FOR ADVANCED SIGE AND Ge MOS AND FIN-FET

先進矽鍺及鍺金氧半與鰭式場效電晶體之閘堆疊製程研究

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-007.

*This study also received supports from TSRI, and NSTC .

Introduction

With the development of Moore's Law, germanium with high carrier mobility has been regarded as one of the highest potential solutions to speed up the technology node. However, the germanium material still has some issues to be overcome.

Germanium has, poor interface quality and insufficient thermal stability which may result in degradation of device characteristics. In this project, some novel process techniques are proposed to improve the characteristics of Ge CMOS FinFET, such as post-plasma, and supercritical fluid oxidation treatments. The interface layer in gate stack is subjected to a post-plasma nitridation (PPN) and oxidation (PPO) treatment to suppress the formation GeOX and eliminate interface defects. The interface layer in gate dielectric layer is passivated by a supercritical fluid (SCF) process. Thanks to the reduced oxygen vacancy content and low oxidation state, the overall quality of gate stack can be optimized.

For the future study, a vacuum annealing process, which can attract interface defects upward to the boundary, may assist the subsequent low-temperature post-oxidation process. Defects can be more effectively minimized, such as passivation of the gate stack, suppression of the thickness increase of the interface layers, and reduction of oxygen vacancies.

Conclusion

With analysis(XPS), both PPO+SCF and PPNO+SCF samples reduce the oxygen vacancy value.

The PPNO+SCF sample shows better CV and dispersion characteristics and a EOT of 0.67 nm.

The Jg of the device with PPNO+SCF is similar and shows lower Dit of p-sub Ge MOS device.

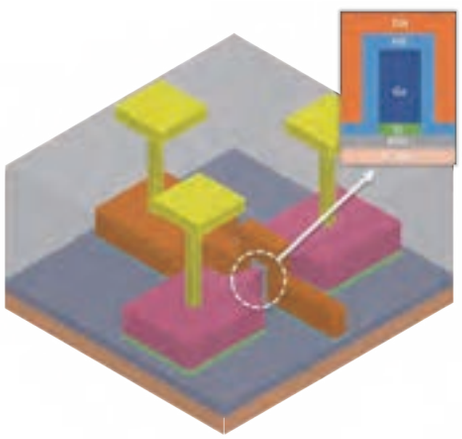
Device with PPNO+SCF exhibits a S.S. of 105 mV/dec, a on/off current ratio of 5.57 order.

After the FN stress reliability test, the degradation of electrical properties in PPNO+SCF sample is minor.

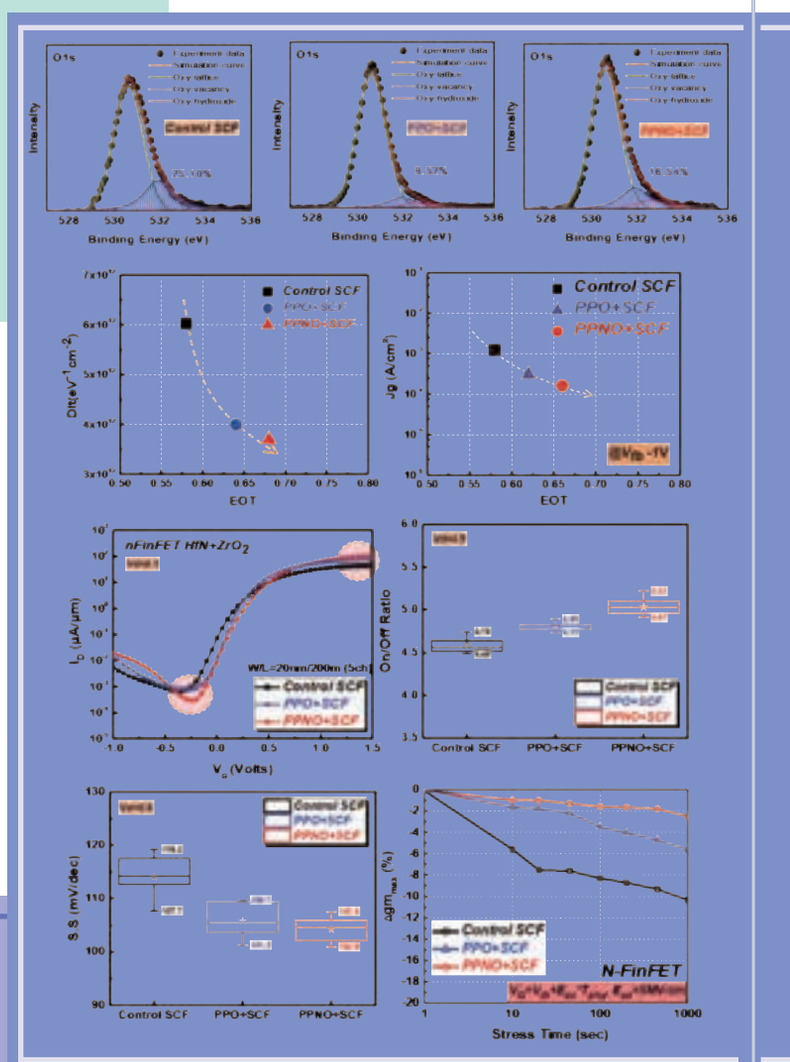
RESULTS

Ge n-FinFET with in-situ plasma in ALD and SCF treatments on gate stacks

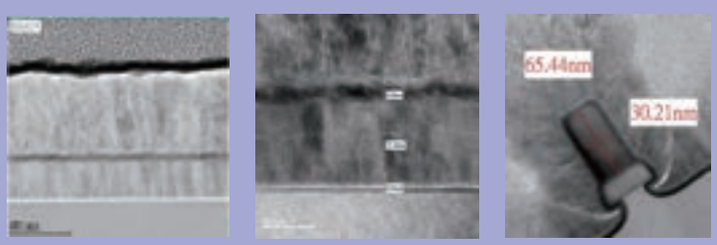
ID	Sub	BL	HK	PPN	PPO	Cap	SCF	Metal Gate	IMP	PMA
Control SCF				x	x					
PPO+ SCF	Ge SOI	HfN 1nm	ZrO_2 3nm	x	O_2 plasma	TiN 2nm	SCF H_2O_2	TiN 100nm	BF2 1E15 10keV	MWA 2.75P 100s
PPNO+ SCF				NH_3 plasma	O_2 plasma					



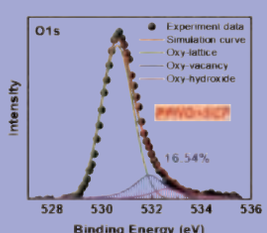
1. Ge epitaxial layer on SOI
2. Active Region definition
3. RTO 400°C 1min
4. Wafer clean process 2% HF 60s
5. HfN/ZrO_2 Layer formed by ALD
6. In-situ O_2 plasma (PPO)
7. In-situ NH_3 +O_2 plasma(PPN+PPO)
8. TiN capping layer formed by ALD
9. SCF treatment (H_2O_2 100°C, 3000psi)
10. TiN 1000Å deposited by sputter
11. Gate etching
12. Imp. Area definition
13. S/D Imp. By P^{31+} 1x10^{15} cm^{-2}10keV
14. MWA at 2.75 P for 100 s
15. TEOS-2000Å deposited by PECVD
16. Contact hole formation
17. Al-Cu 3000Å deposited
18. Metal Pad definition

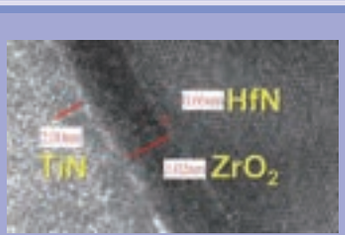


MATERIALS & METHODS



STEM IMAGE





Discussion

A very small content of oxygen vacancy is obtained with a PPNO+SCF treatment.

Both PPO and SCF treatment can effectively reduce oxide vacancy.

The oxygen vacancy decreases from 25.1% to 9.5%, showing more than 2.5 times.

The Dit values in PPN+PPO sample are the lowest.

The variance of data for all samples is quite small.

The lowest S.S. value of 104 mV/dec and best reliability are achieved with PPN+PPO.

National Tsing Hua University

Wu, Yung-hsien

INTEGRATING ADVANCED PROCESS AND MATERIAL ANALYSIS TECHNOLOGY TO IMPLEMENT HIGH-PERFORMANCE/HIGH-RELIABILITY FERROELECTRIC MEMORY BASED ON P-TYPE OXIDE SEMICONDUCTOR

整合先進製程與材料分析技術實現基於P型氧化物半導體之高效能/高可靠度鐵電記憶體

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Research Team:

Chun-I Kuo, Kai-Sheun Lee, Yi-Fan Chen

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-008

*This study also received supports from TSRI, and NSTC

Introduction

To address the demand of enabling both training and inference tasks in the edge accelerators for AI applications, it has become essential to explore new memory technologies and monolithic 3D integration. These advancements aim to embed dense memory into the edge accelerator while directly implementing In-Memory-Computing (IMC) beyond conventional von-Neumann architecture.

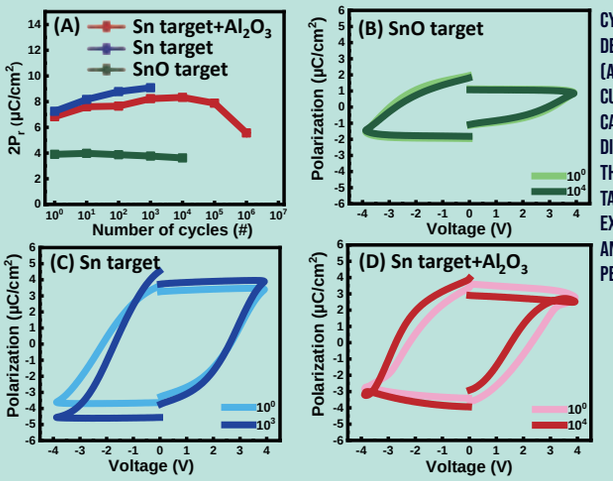
HfO_2-based ferroelectric field effect transistors (FeFETs) is promising for IMC applications. To implement monolithic 3D chips, developing BEOL compatible oxide semiconductor as the channel material for memory circuits is indispensable. Currently, all related researches have been limited to n-type oxide semiconductors such as IGZO, IWO, or ZnO as channel materials, with a lack of investigation into p-type oxide semiconductors.

The objective of this project is to develop p-type oxide semiconductor SnO as the channel for $HfZrO_x$ (HZO)-based p-FeFETs. This not only provides another potential option for monolithic 3D chip technology but also allows for the integration of more diverse circuit functions with n-FeFETs.

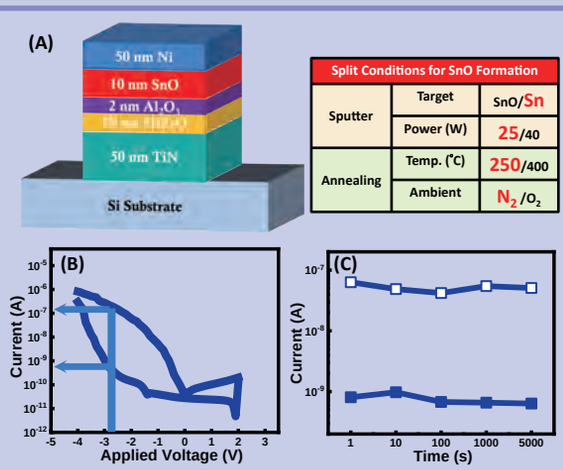
Conclusion

Various processes conditions were extensively explored to develop p-type SnO oxide semiconductor for HZO-based ferroelectric memory and the optimal condition has been confirmed by physical analyses. Additional Al_2O_3 has been introduced between SnO and HZO to alleviate Zr and Sn inter-diffusion. With the best process conditions, the FE capacitors show the highest P_r, most robust endurance up to 10^6 cycles, FTJ memory with high ON/Off ratio and good retention. The research results pave another avenue to implement monolithic 3D memory.

RESULTS



CYCLING NUMBER DEPENDENT (A) $2P_R$ AND (B-D) P-V CURVE FOR FE CAPACITORS WITH DIFFERENT CONDITIONS. THE CAPACITORS WITH Sn TARGET AND Al_2O_3 EXHIBIT THE HIGHEST PR AND BEST ENDURANCE PERFORMANCE.



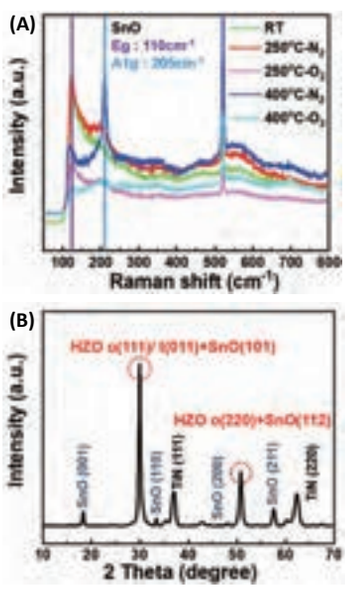
Split Conditions for SnO Formation		
Sputter	Target	SnO/Sn
	Power (W)	25/40
Annealing	Temp. (°C)	250/400
	Ambient	N_2 /O_2

(A) STRUCTURE AND SPLIT CONDITIONS FOR FE CAPACITORS (OPTIMAL CONDITION IS HIGHLIGHTED).

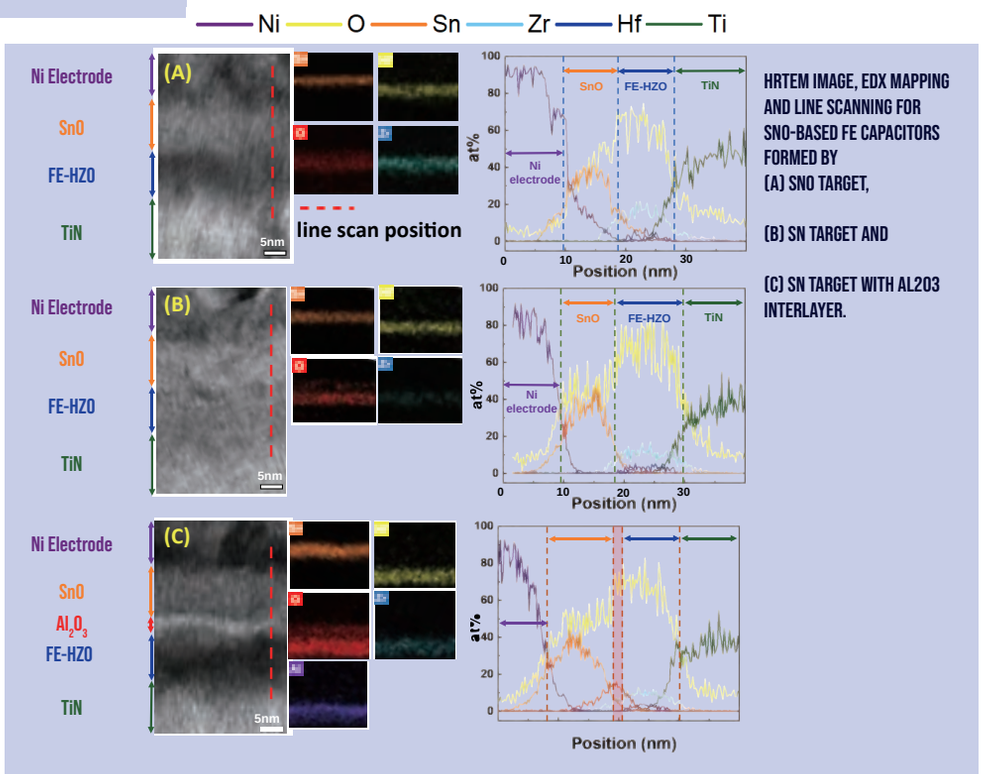
(B) I-V CURVE OF FTJ MEMORY WITH HIGH ON/OFF RATIO (~100 @ -2.8 V).

(C) RETENTION OF ON/OFF STATE.

MATERIALS & METHODS



(A) RAMAN SPECTRUM AND (B) GIXRD PATTERN FOR SNO-BASED FE CAPACITORS FORMED BY SN TARGET. 250 °C ANNEALING IS MORE FAVORABLE TO FORM P-TYPE SnO REGARDLESS OF O_2 OR N_2 AMBIENT.



HRTEM IMAGE, EDX MAPPING AND LINE SCANNING FOR SNO-BASED FE CAPACITORS FORMED BY (A) SNO TARGET,

(B) SN TARGET AND

(C) SN TARGET WITH AL203 INTERLAYER.

Discussion

The optimal process conditions to form p-type SnO oxide semiconductor are obtained by PVD deposition using Sn target under 25 W with subsequent 250 °C annealing in N_2 ambient which is evidenced by Raman spectroscopy and GIXRD analysis. With additional Al_2O_3 interlayer between HZO and SnO, inter-diffusion of Zr and Sn can be alleviated which is confirmed by EDX analysis. The optimal process condition also makes the highest P_r (~10 μC/cm²) for FE capacitors and the higher P_r at negative bias attests to the p-type nature of the film due to accumulation effect. The devices show endurance up to 10^6 cycles, FTJ memory with high ON/OFF ratio (~100) and desirable retention as well, opening up a new opportunity for memory application.

National Tsing Hua University

Chen, Chien-chun

SOFTWARE DEVELOPMENT FOR ELECTRON MICROSCOPE IMAGE AUTOMATIC MEASUREMENT

電子顯微鏡影像自動量測軟體開發

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-009.

Introduction

目前電晶體的臨界尺寸量測是由FIB製備薄片樣品後由TEM進行拍攝，尺寸量測則需由人工進行。當需要量測大量的影像，就需要自動化的量測軟體來完成這些機械化的動作。目前閎康科技是與供應商合作，在供應商的軟體平台上進行自動化量測與輸出。一旦出現影像變異過大，供應商的軟體就會出現無法正確提供量測的狀況，閎康科技無法自行處理(修改內部程式)，需仰賴與供應商的來回溝通以修正軟體。當量測問題產生在下班時間時，供應商就無法即時回應的狀況。

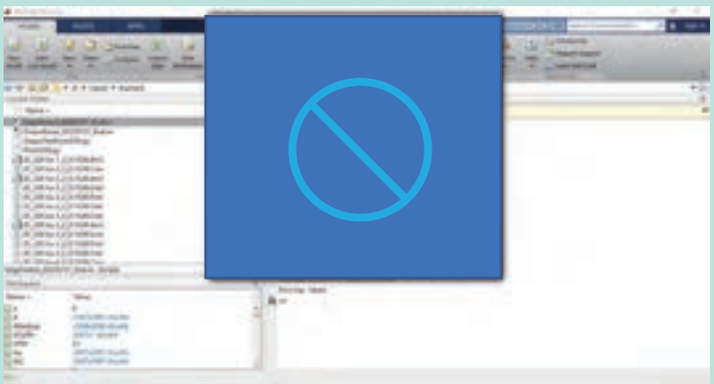
本計畫的目標即為解決閎康科技在自動化量測上面臨的問題。
解決方案分短期與長期：
短期：利用市面上常用的軟體開發自動量測系統(以本實驗室使用MATLAB為例)，此量測系統量測完所有需求輸出到文字檔。接下來將量測結果自動化輸入TEM最廣泛使用的DigitalMicrograph® (DM)軟體。如此即便軟體無法提供100%正確量測，可以人工方式進行修補，以利快速回覆委測案件。
長期：本實驗室與閎康科技共同培養博士生，這些博士生持續開發自動量測系統相關模組。

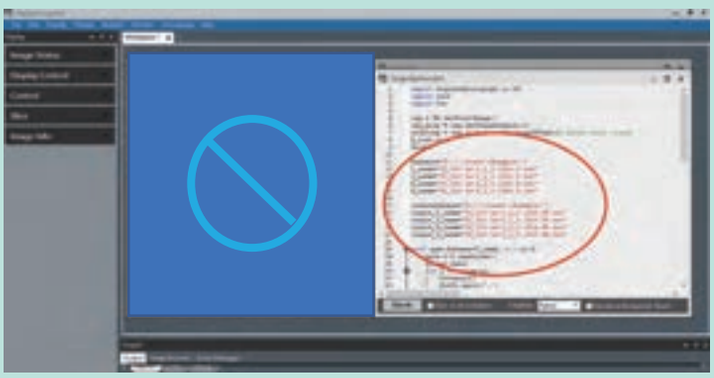
未來這些學生進入閎康科技成為IT人才，對所開發的軟體不僅熟悉，亦能自行使用與持續拓展自動量測模組，對各種差異極大的影像可搭配不同模組進行量測，完全自己自足無需等待供應商提供修正軟體。

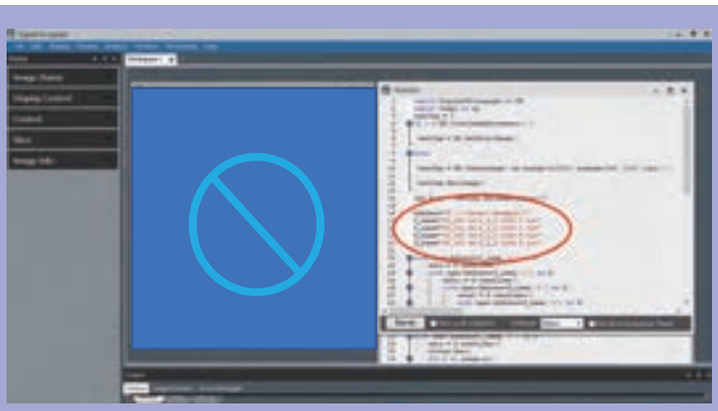
Conclusion

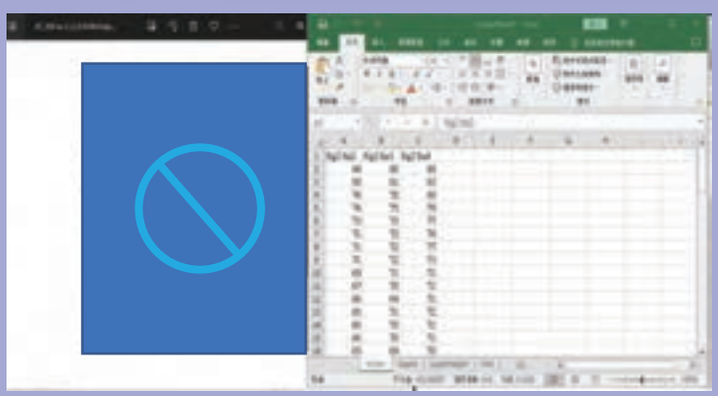
完成短期解決方案之關鍵模組。在閎康科技提供約600張暗場影像中，完成指定量測。只要執行提供的程式(m & py 檔案)與TEM影像(dm3 檔)放在同一個資料夾就可以直接執行量測繪圖、手動修改量測線段與輸出Excel分類檔案。

RESULTS



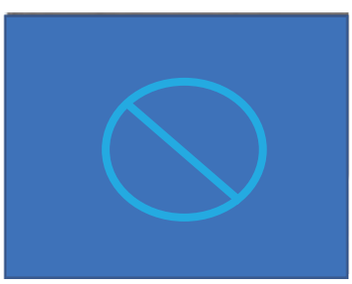


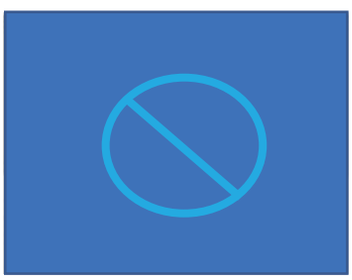


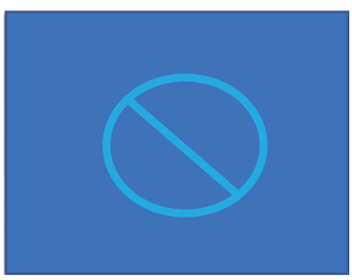


(左上)在MATLAB環境中執行EdgeDetect.m，即可對ISO之外的dm3進行量測，量測線段繪於figure內，同時輸出線段的txt檔。(右上)若對量測結果需要個別進行線段調整，將該dm3檔與PlotInDM.py以及OutputTextFromDM.py拖曳入DM軟體。這裡以ZC_320kx-2_2_0.1528.dm3為例。將PlotInDM.py修改對應的txt檔(如紅圈)再執行，即可在DM內進行繪製線段。(左下)假設要手動修改線段，如該紅圈處的黃線為新修正線段，則在修改完後，在OutputTextFromDM.py內修改儲存txt檔並執行，即產生新的txt檔。(右下)最後在MATLAB環境中執行OutputExcel.m則可對所有新的txt檔匯出excel檔與圖檔。

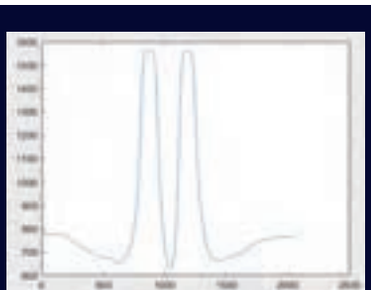
MATERIALS & METHODS

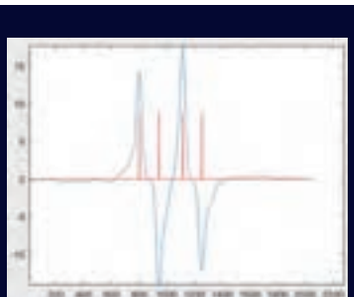


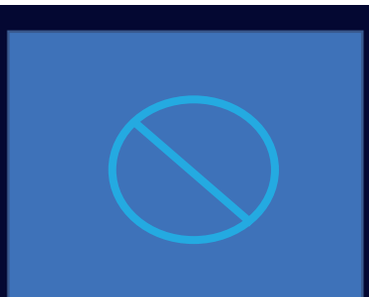




模組一：利用高通濾波在傅立葉空間將低頻區域濾除，得到對比提高影像。下圖由左而右依次為原圖、去背景、高通濾波。影像對比也由左至右逐步明顯，同時可針對不同結構進行尺度偵測。







模組二：將方才高通濾波影像沿列方向疊加，可中間圖示的一維曲線分布。將該一維曲線進行邊界分析，可得到四個邊界(如圖中的紅線)，其中兩兩定義一根鰭的左右邊界。

欲量測各種關鍵尺寸，僅需要搭配模組一與二，從原圖、去背圖或高通濾波圖中選取直線或橫線進行邊界判讀，即可完成如右下圖一般的各式量測。

National Tsing Hua University

Chen, Tsan-yao

次奈米金屬-氧化物半導體異質接合於高溫還原氣氛下結構演繹行為分析技術

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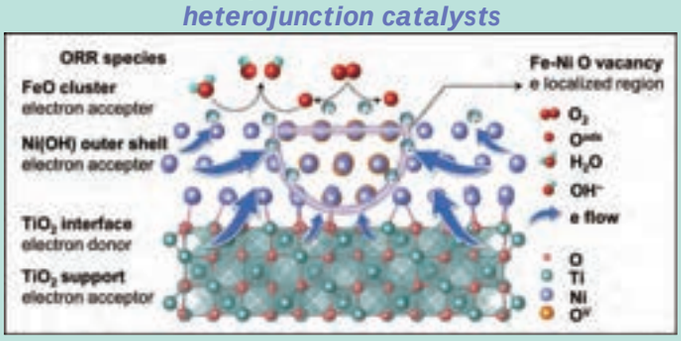
This study is supported by Materials Analysis Technology Inc. under contract 2022-T-010.

*This study also received supports from National Synchrotron Radiation Research Center (NSRRC), and NSTC.

DENSITY FUNCTIONAL THEORY PREDICTED THAT THE ACTIVITY OF NANOPARTICLES IN OXYGEN REDUCTION REACTION CAN BE MANIPULATED VIA CONTROLLING THEIR HETEROATOMIC AND THE SURFACE DIPOLE CONFIGURATIONS.

Catalyst Design Rules

New concept: subnano-metal/oxide heterojunction catalysts



Summary

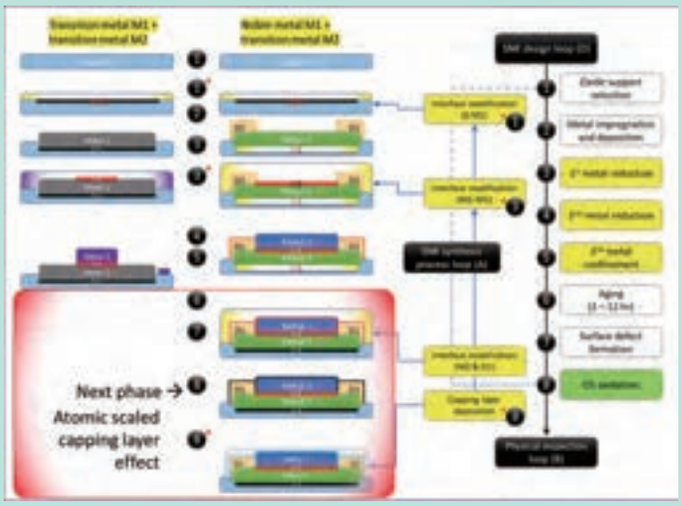
single nanoparticle reactor (SNR) comprising TiO_2 supported metal / metal oxide nanoparticle (NPs) and atomic cluster decoration are developed in this project.

(Ni - Fe) decorated SNR, the CH_4 production yield and selectivity are respectively improved by ~90% and 15% by decorating 5 wt% of Fe in the Ni@TiO_2 surface.

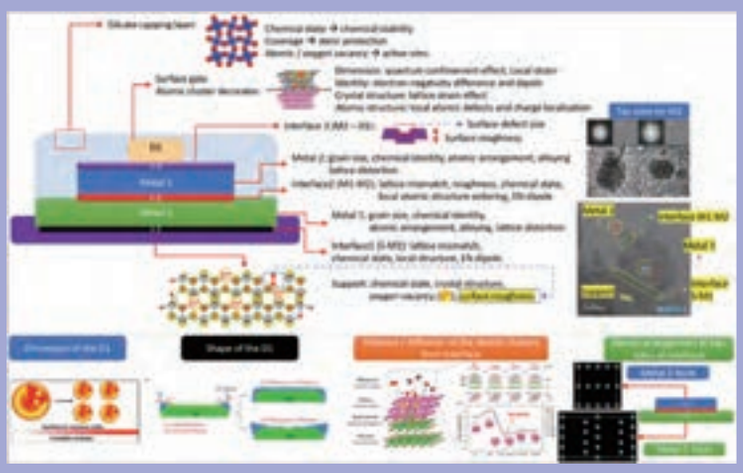
The NiFe-5 is a TiO_2 supported NiFeOx NPs with high contents of oxygen vacancy in mix oxide. In-situ XAS results elucidate that the improvement is attributed to the collaboration between OV and the neighboring Fe, Ni atoms. An exceptional stability in the thermal cycle test is demonstrated due to the facilitated redox kinetics.

SYNTHETIC PROCESSES AND BOTTLENECKS OF HIERARCHICAL METAL OXIDE SUPPORTED NANOPARTICLE

Synthetic Processes



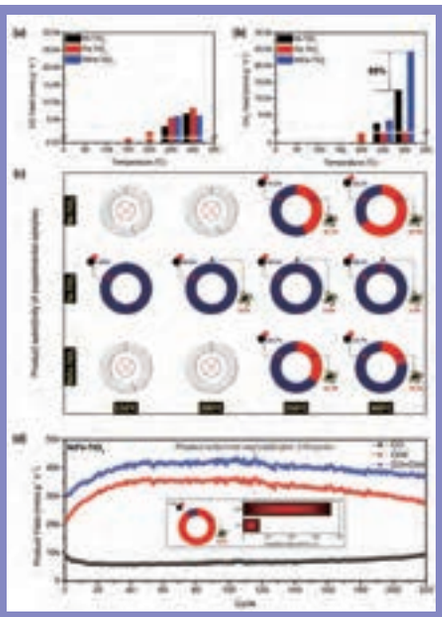
Bottlenecks



SEMICOHERENT INTERFACE SUPPRESS THE STABILITY OF METAL-OXIDE SUPPORTED NPS IN CHEMICAL REACTION

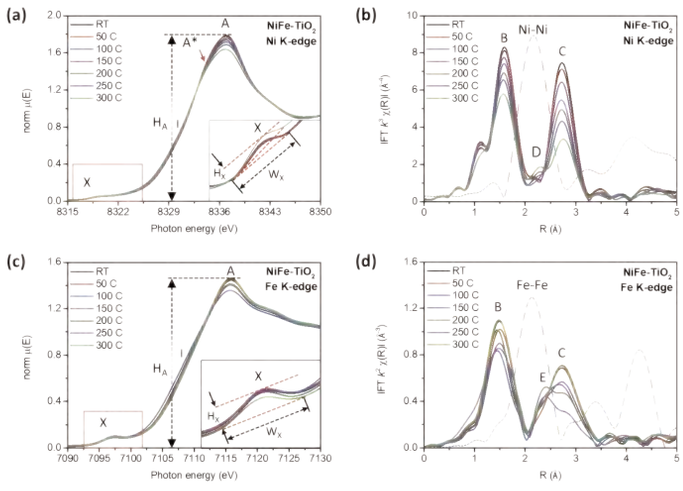
RESULTS & DISCUSSION

CO_2 Methanation Performance



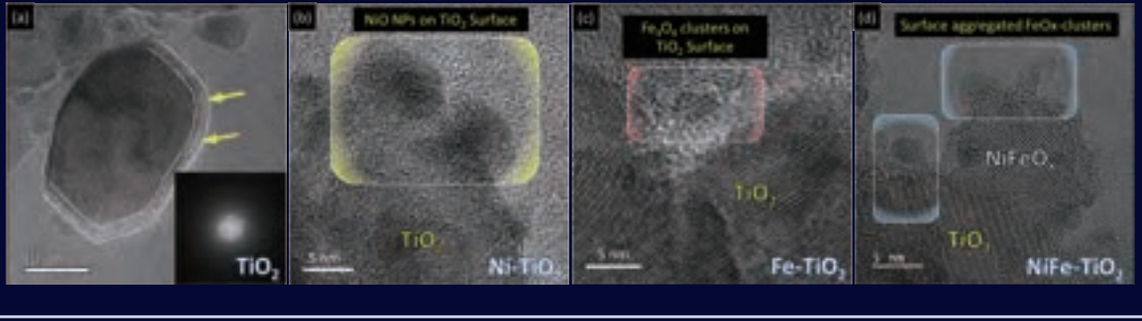
(A) CO AND (B) CH_4 PRODUCTION YIELD OF TIO2 SUPPORTED FENIOX NPS IN CO_2 METHANATION REACTION. (C) CORRESPONDING SELECTIVITY OF PRODUCTS AT SELECTED TEMPERATURE AND (D) THERMAL CYCLE TEST RESULTS IN CO_2 METHANATION AMBIENT.

Physical Structure Inspections



IN-SITU X-RAY ABSORPTION NEAR-EDGE STRUCTURE (XANES) AND FOURIER TRANSFORMED EXTENDED X-RAY ABSORPTION FINE STRUCTURE (EXAFS) SPECTRA OF NIFE-TIO2 AT Ni (A) AND (B) AND Fe (C) AND (D)) K-EDGE. THE AMBIENT ENVIRONMENT IS A MIXTURE OF H_2 AND CO_2 GASES (H_2 : CO_2 = 3 : 1) IN THE FLUX OF 20 SCCM WITH THE TEMPERATURE RANGING FROM 30 (RT) TO 300°C.

HRTEM IMAGES OF THE (A) TiO_2, (B) Ni-TiO_2, (C) Fe-TiO_2 AND (D) NiFe-TiO_2 SAMPLES.



National Tsing Hua University

Duh, Jeng-gong

ENHANCING THE RELIABILITY OF MICRO-BUMPS AND BGA BUMPS BY NOVEL UBM ALLOY DESIGN WITH THE ADDITION OF Ni AND Zn

通過添加 Ni 和 Zn 的新型合金設計提升微凸塊錫點和球狀陣列凸塊錫點的可靠性

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-011.

*This study also received supports from NSTC.

Introduction

For the advanced 2.5D/3D IC applications, the IMCs suppression and phase stability should be emphasized. With a reduced size of micro-bumps, the IMCs would occupy a high volume fraction of the joints during the reflow process or operation. A high volume fraction of IMCs and excessive phase transition could induce internal stress and voids, which might be adverse to reliability of interconnection.

The addition of Ni and Zn was reported to enhance the phase stability of hexagonal η-Cu_6Sn_5, which inhibited the volume change caused by phase transition and internal stress. Moreover, the grain refinement strengthening also achieved by the addition of Ni and Zn. The Cu_3Sn phase was accompanied with formation of Kirkendall voids, and it can be also suppressed by element doping.

For the BGA joints, low-temperature solder is important for the reduction of warpage. Sn-58Bi is one of most popular low-temperature solder. However it was criticized for its brittleness. The different solubility of Bi in Cu_6Sn_5 and Cu_3Sn leads the Bi segregation between the Cu_3Sn layer and UBM. Co-addition of Ni and Zn in UBM was expected to inhibit the Cu_3Sn completely and suppressed IMCs formation considerably.

Conclusion

The orbital interaction of Cu–Zn is much stronger than that between Cu–Cu, which retards the Cu dissolving from the Cu–Zn based substrate into solder to form the IMCs.

The co-addition of Ni and Zn retarded the formation of Cu3Sn phase, which also inhibited the volume shrinkage , internal stress and void formation.

The findings in this work is expected to enhance the reliability of joints under long-term operation.

RESULTS

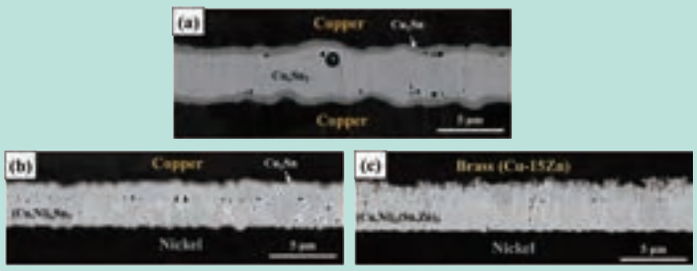

FIGURE1. BEI OF (A)Cu/Sn-3.5Ag/Cu, (B) Cu/Sn-3.5Ag/Ni, AND (C) Cu-15Zn/Sn-3.5Ag/Ni (REFLOWED AT 260°C FOR 300 SECONDS)

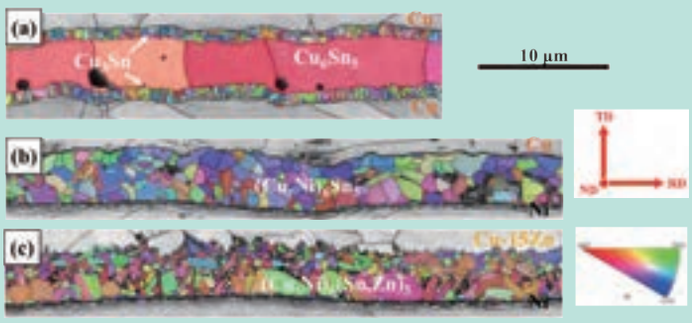

FIGURE2. BAND CONTRAST MAPPING OF (A)Cu/Sn-3.5Ag/Cu, (B) Cu/Sn-3.5Ag/Ni, AND (C) Cu-15Zn/Sn-3.5Ag/Ni BY EBSD

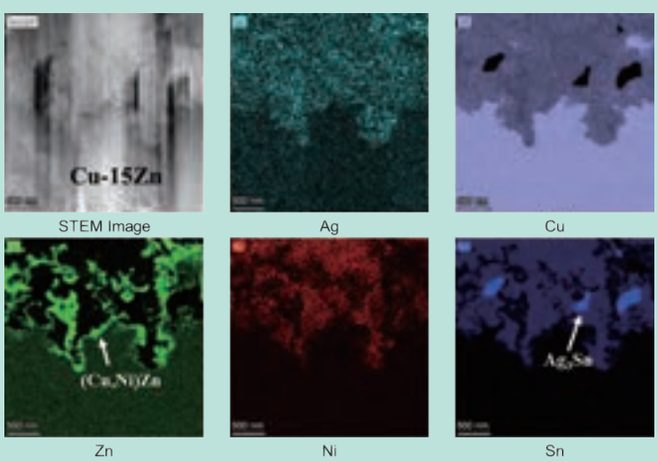

FIGURE3. ELEMENTAL MAPPING OF Cu-15Zn/Sn-3.5Ag/Ni SAMPLES AND THE OBSERVATION OF ZINC-RICH LAYER BY TEM/EDS

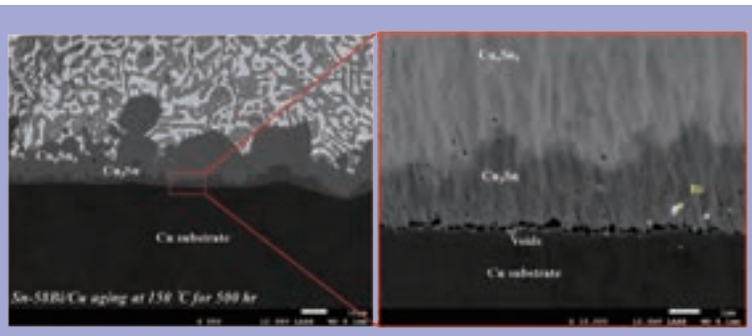

FIGURE4. BEI OF Sn-58Bi/Cu BGA JOINT AND BISMUTH/VOIDS BETWEEN Cu3Sn LAYER AND CU SUBSTRATE

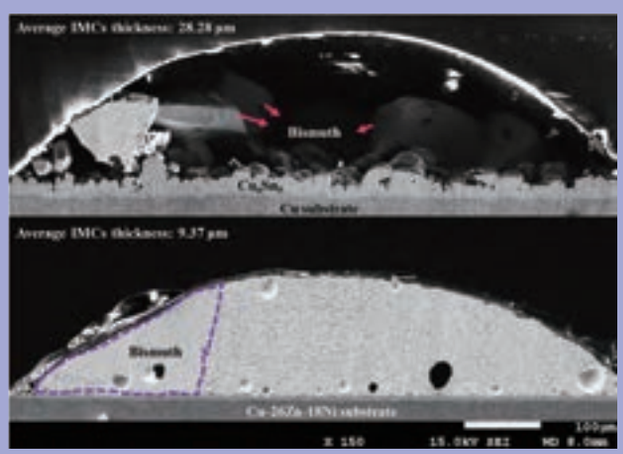

FIG.5 BEI OF Sn-58Bi/Cu, AND Sn-58Bi/Cu-26Zn-18Ni AFTER ISOTHERMAL AGING AT 150°C FOR 1000 HOURS

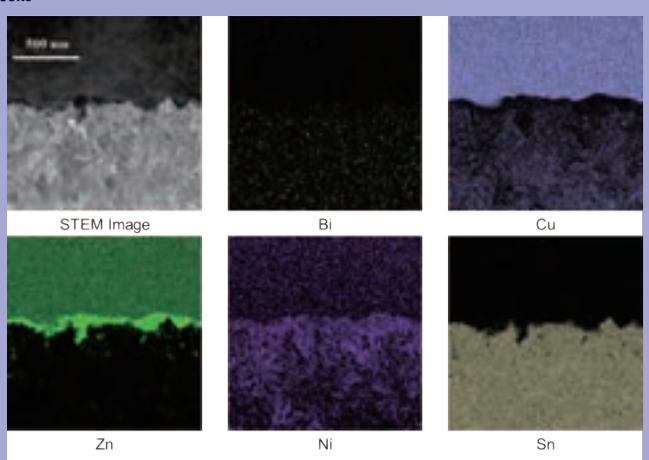

FIG.6 ELEMENTAL MAPPING OF Sn-58Bi/Cu, AND Sn-58Bi/Cu-26Zn-18Ni AFTER ISOTHERMAL AGING AT 150°C FOR 1000 HOURS BY TEM/EDS.

Materials & Methods

The Cu15Zn/Sn-3.5Ag/Ni micro- bumps formed a Zinc-rich phase in cluster and layer shape around the Cu-Zn substrates.

The Sn-Bi/Cu-26Zn-18Ni exhibited a considerable IMCs suppression effect, which was due to the formation of the Zinc-rich phase.

The as-mentioned Zinc-rich phase was hard to identify by EPMA due to the limitation of spatial resolution

The FIB processing with TEM/EDS service by MA-tek provides strong assistance for this work.

Discussions

The addition of Ni layer and Cu-Zn substrates modified the grain texture and grain size significantly, which was expected to enhance the mechanical reliability of sub-micro solder joints.

The IMCs thickness in Sn-58Bi/Cu-26Zn-18Ni joints was only 1/3 of that in Sn-58Bi/Cu joints after 1000 hours of thermal aging, which is favorable for the reliability under long-term operation.

The co-addition of Ni and Zn enhances the phase stability of hexagonal η-Cu_6Sn_5. The phase transition to Cu_3Sn phase was inhibited in micro-bumps or BGA joints in this work

National Tsing Hua University

Fang, Wei-leun

DEVELOPMENT AND PERFORMANCE VERIFICATION OF MICRO PIEZOELECTRIC TRANSDUCERS TESTING TECHNOLOGY

微型壓電傳感器測試技術之開發及性能驗證

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-012.

*This study also received supports from NSTC, and TSRI.

Introduction

近年來隨著消費性電子產品的爆發性成長，人工智慧結合物聯網(AIoT)等技術，大量微型傳感器(感測器與致動器)已被廣泛使用在不同的應用領域，其中壓電薄膜材料已迅速切入半導體與微機電領域。目前全球許多公司已緊鑼密鼓地投入壓電薄膜傳感器相關技術的開發，而壓電薄膜的製備以及其重要材料參數萃取，是亟待建立的核心技術，且有一定的門檻。

因此，清大方維倫教授的研究團隊MDL(Micro Devices Lab)希望透過閎康在測試上的基礎，共同開發及建立壓電薄膜和元件的量測技術，協助串聯國內業者，實現壓電平台的產業鏈結，並攜手合作切入新型商業應用市場。透過閎康科技專業的材料檢測技術與設備，和MDL微傳感元件測試經驗，本計畫已獲致壓電薄膜與致動器之關鍵成果。

Publications

H.-Y. Lin, et al., Transducers 2023, Kyoto, Japan.
T.-C. Wei, et al., Transducers 2023, Kyoto, Japan.
C.-C. Hsu, et al., Transducers 2023, Kyoto, Japan.
專利:中華民國2篇(申請中) 美國2篇(申請中)

Conclusion

壓電薄膜為極具應用潛力之功能性薄膜

清大MDL完成壓電薄膜元件開發與功能測試，並在閎康協助下完成壓電薄膜性質檢測

壓電薄膜性質: 壓電係數 (54 pm/V)、極化特性、環境影響評估、偏壓效應等等

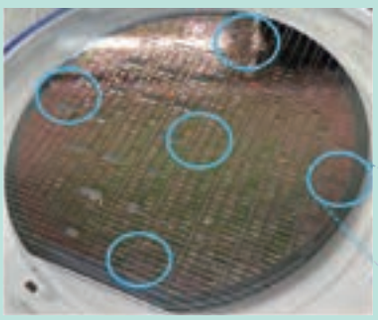
壓電薄膜元件:
+ 壓電微型光掃描面鏡: 高頻、大角度旋轉，作為LiDAR, AR HUD的應用
+ 壓電微型聲學致動器: 入耳式高頻揚聲器

結論: 清大MDL與閎康的合作，為壓電薄膜商品化應用，建立關鍵的核心技術

Wetting Angle on Cu

PIEZOELECTRIC MATERIAL PROPERTIES

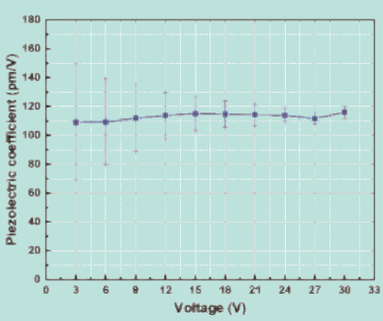
Piezoelectric material properties extraction

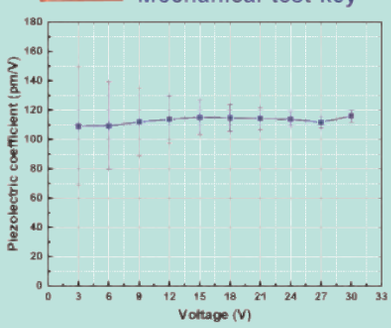


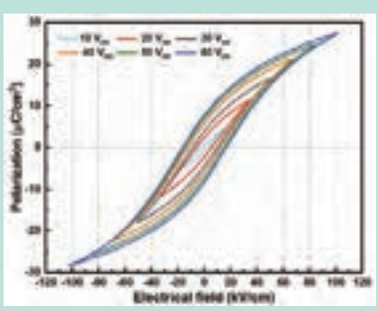
Electronic test key

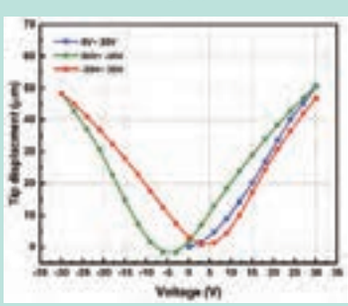
Test keys distributed on wafer

Mechanical test key

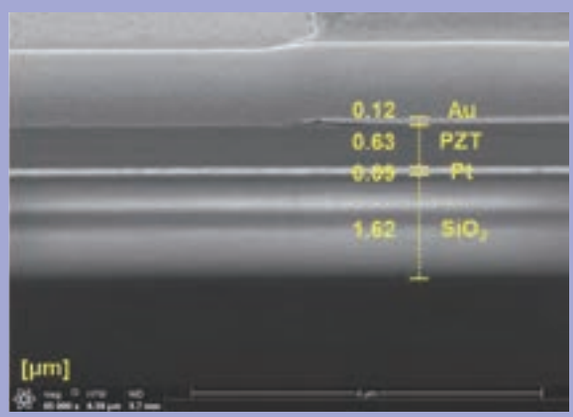




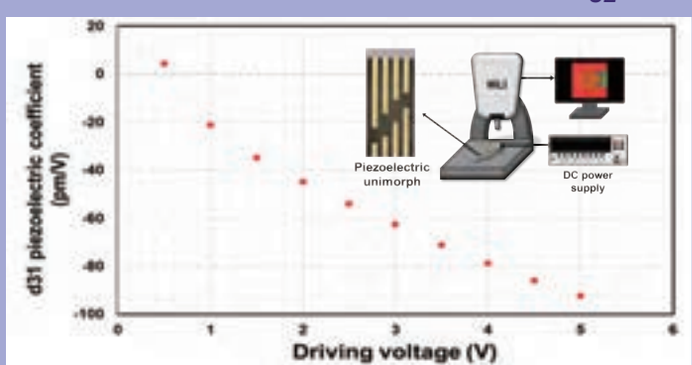




Piezoelectric material layer



Piezoelectric coefficient d_{31}

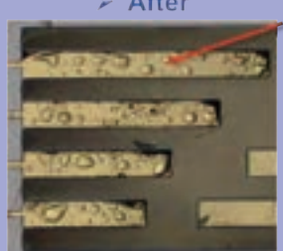


Environmental test

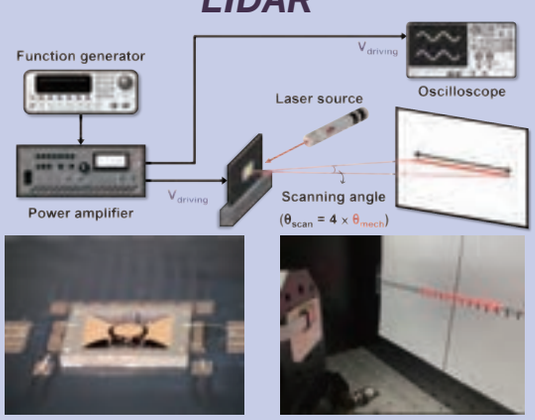
Before

After

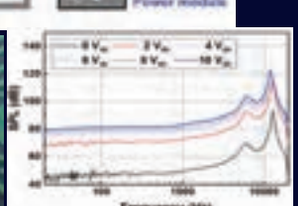
Bubble



LiDAR



ACOUSTIC TRANSDUCER



National Tsing Hua University

Chiu, Po-wen

GATE DIELECTRICS INTERFACE FOR 2D FETS BEYOND N1.5

N1.5技術節點下二維電晶體之閘極氧化層界面研究

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-013.

*This study also received supports from NSTC.

Introduction

In recent years, a newly emergent 2D material of Bismuth Oxyselenide (Bi2O2Se) has garnered great attention due to its high electron mobility and intriguing native oxide which possesses high-quality dielectric interface. This new 2D semiconductor asserts its supremacy over alternate 2D materials. Here, we present synthesis of Bi_2O_2Se and its oxide form β-Bi_2SeO_5 with a dielectric constant of ~20. The oxidation is achieved through a UV-assisted intercalative oxidation of the Bi2O2Se semiconductor.

In a bid to showcase the scalability prowess of Bi_2SeO_5 in the capacity of gate dielectrics, we meticulously engineer top-gated Bi_2O_2Se FETs, wherein the pivotal role of gate oxide is impeccably undertaken by Bi_2SeO_5. Evident in the device metrics are Ion/Ioff ratio of over 107 and field-effect mobility measuring over 1347 cm^2 /Vs, a subthreshold swing of less than 148 mV/dec, and a conspicuously high breakdown voltage exceeding 10^7 V/cm.

Intrinsic to the device architecture are noteworthy parameters such as extra-low gate leakage, and the overall interface trap density Dit, which approximates ~10^{11} 1/cm2eV. These metrics collectively serve as fundamental benchmarks, holding pertinence for the evaluation of emergent technologies in a broader context.

Conclusion

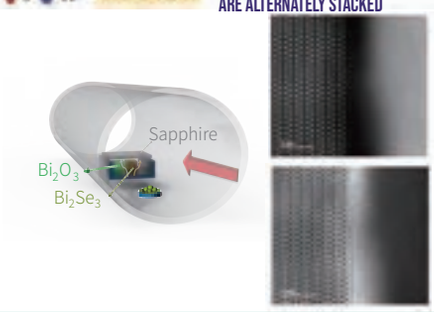
The presented 2D Bi_2O_2Se field-effect transistor with epitaxial high-k Bi2SeO5 dielectric satisfy the most stringent requirements for future advanced transistors, including atomically flat gate interface, high carrier mobility, and high drive current density. The high carrier mobility is attributed to high quality single crystalline Bi_2O_2Se, low metal contact resistivity, low interface defects, and a high-quality native oxide layer. With further optimization to achieve precisely site-specific growth of high-density 2D oxide heterostructure arrays on industrial-compatible dielectric substrates will enable further transistor scaling and could extend Moore's law.

RESULT & ANALYSIS

Structural Properties of Bi_2O_2Se

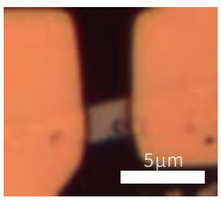
Bi_2O_2Se IS A SINGLE-CRYSTALLINE LAYER MATERIAL WITH TETRAGONAL CRYSTAL STRUCTURE AND SPACE GROUP SYMMETRY I4/MMM

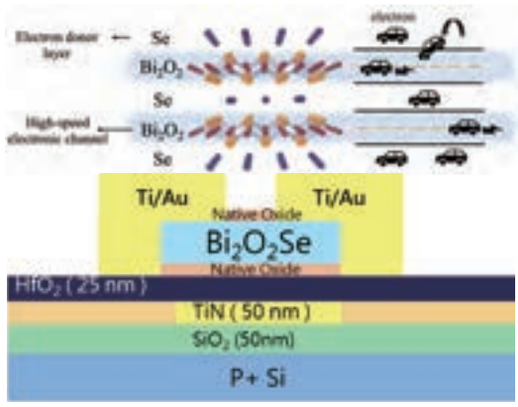
POSITIVELY AND NEGATIVELY CHARGED LAYERS ARE ALTERNATELY STACKED

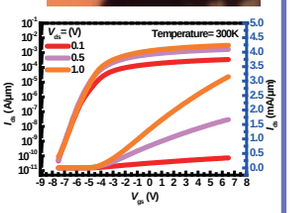


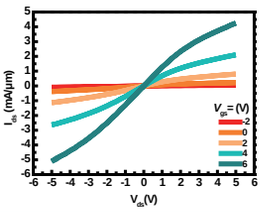
Bi_2O_2Se/Bi_2SeO_5 FET for stacking technology and application:

I_{on}/I_{off} ratio	10^7
Mobility	1347 $cm^2/V{\cdot}s$
On Current	3×10^{-4} A/μm
SS	~370 mV/dec
V_{th}	~ −2.15 V

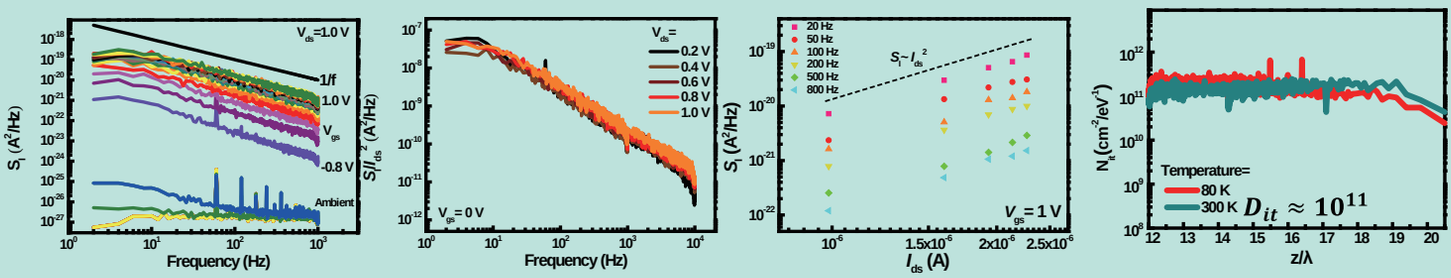




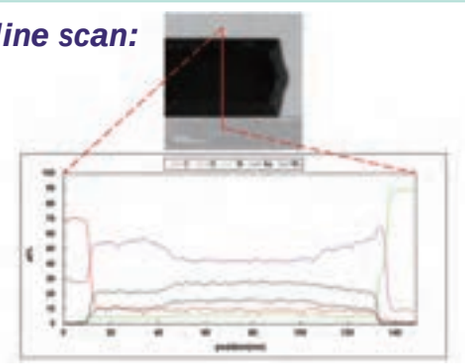




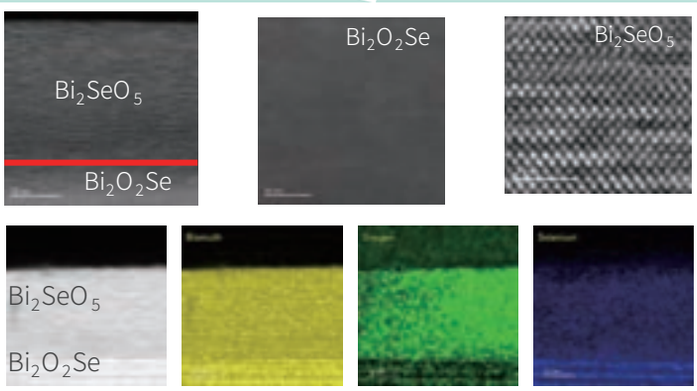
Low-frequency Noise Analysis for D_{it}:



EELS line scan:



TEM:



Methods

We use UV-assisted oxidation at 150℃ to synthesize a uniform high-k single-crystalline native oxide Bi_2SeO_5 on the high-mobility 2D semiconducting Bi_2O_2Se.

Low-frequency noise measurement is applied to measure total interface trap density D_{it} between the oxide and semiconductor.

Etching of the contact area with argon ion source was performed before metal deposition to increase carrier injection.

National Yang Ming Chiao Tung University

Wu, YewChung Sermon

ANALYSIS OF SURFACE DAMAGE LAYER AND ITS IMPACT ON 4H-SIC EPITAXIAL LAYER BY USING HIGH-RESOLUTION EBSD

以HR-EBSD分析SiC晶片表面損傷層與對4H-SiC磊晶的影響

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Tsan Feng Lu, Hong Jun Huang

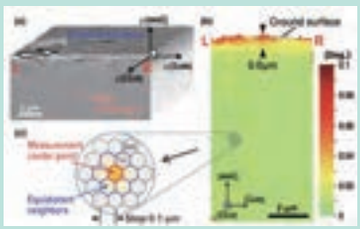
This study is supported by Materials Analysis Technology Inc. under contract 2022-T-014.

Reference:
[1] Tsukimoto, Susumu, et al. "Local strain distribution and microstructure of grinding-induced damage layers in SiC wafer." Journal of Electronic Materials 47.11 (2018): 6722-6730.

Introduction

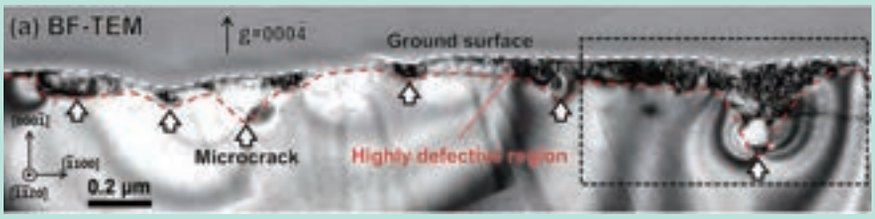
SiC的超硬度、脆性，使晶片在「切磨拋」的過程中，非常不容易控制。很容易就會有損傷層特別是局部應變（strain）的殘留。這將會影響之後磊晶層的品質。

在各種損傷層分析法中，TEM與HRTEM最準確。但觀察區域小，試片製備（FIB）與觀察成本非常高，且速度慢。
EBSD比較經濟，快速且觀察區域大。其中用到 kernel average misorientation (KAM) 的分析法。在不同的SiC表面上磊晶SiC層。分析表面SiC磊晶層與SiC晶片表面損傷層相對應的關係。



4H-SiC (C face)

LIERATURE REVIEW[1]



Methods

4H-SiC 晶圓由標準切割製程所製造:

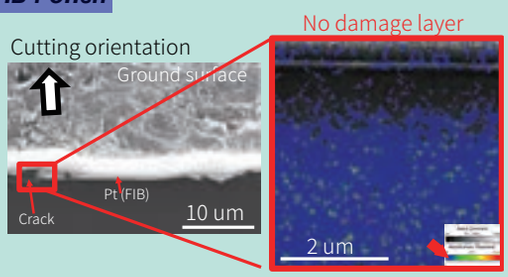
選定晶圓中心位置，進行Si面與C面的剖面EBSD量測
EBSD試片前處理分為 (a) FIB拋光處理及 (b) 裂片後無任何處理
最後用TEM確認Si面與C面的表層下方是否存在損傷層

將4H-SiC基板用KOH蝕刻:

用OM定位缺陷位置
用三種磨拋條件進行表面平坦化，皆為標準製程，分別有：
Sample A:粗磨0.5小時
Sample B:粗磨0.5小時再細拋0.5小時
Sample C:粗磨0.5小時再細拋1小時
隨後進行磊晶，再進行KOH蝕刻，最後用OM找出定位點並分析結果

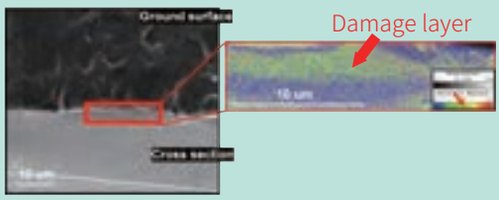
RESULTS

FIB Polish



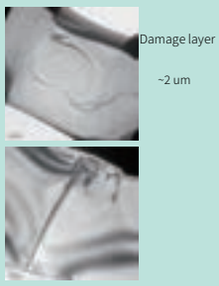
4H-SiC (Si FACE) ON THE WA WAFER

By Cleaving



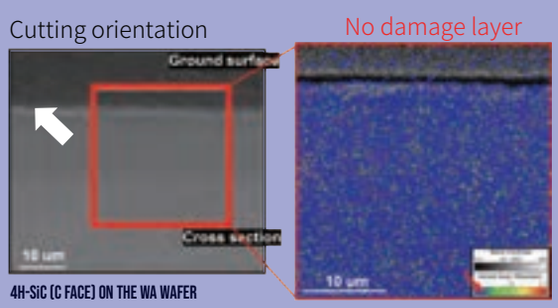
4H-SiC (Si FACE) ON THE WA WAFER

TEM



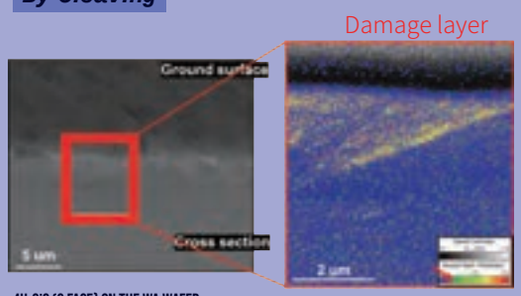
4H-SiC (Si FACE) ON THE WA WAFER

FIB Polish



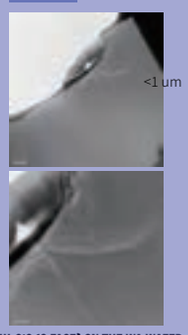
4H-SiC (C FACE) ON THE WA WAFER

By Cleaving



4H-SiC (C FACE) ON THE WA WAFER

TEM



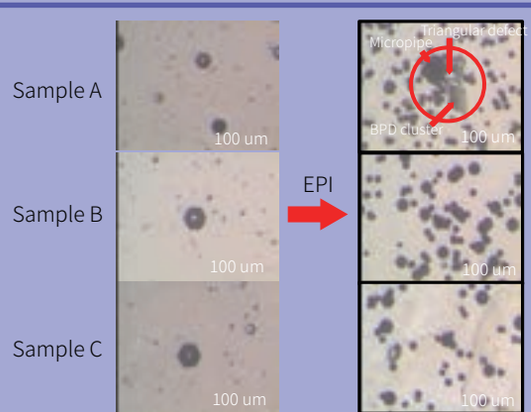
4H-SiC (C FACE) ON THE WA WAFER

TEM Analysis

FIB 拋光後的區域皆無觀察到損傷層。
裂片 (依照文獻及相關專利的製備)，則能夠在表層下方觀察到損傷層。
經由 TEM 量測證實損傷層確實存在，其深度皆大於 1 um。
因此推測 HR-EBSD 所拍攝的損傷層由裂片造成。

OM

	Before EPI (number of defect)	After EPI (number of defect)	Rate (%)
Sample A	42	103	↑145.2
Sample B	40	83	↑107.5
Sample C	38	44	↑ 15.8



Defect Analysis

在As-cut試片中HR-EBSD未觀測應變層，推測經拋光與研磨後的晶片也理應觀測不到。

使用更細緻的拋光處理基板，能有效抑制磊晶後缺陷的形成。

在基板中的BPD缺陷，在磊晶後皆轉變成TED缺陷。

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-015.

INTERFACIAL ANALYSIS OF ULTRA-HIGH-DENSITY INTERCONNECTS

次世代超高密度封裝之介面分析研究

Introduction

Lead (Pb) free solder has been widely used as bonding material in microelectronics packaging known as transient liquid phase diffusion bonding (TLPDB) for the last few decades due to its excellent reliability, process cost, and form factors. To increase the performance of transistors, a larger amount of inputs/outputs (I/Os) is needed, known as Moore´s law. Thus, the dimension of I/Os must be significantly decreased. In addition, solder microbumps have intrinsic issues such as side wall wetting, brittle intermetallic compouds, and bridging, eventually resulting in circuit failures.

Recently, the potential in scaling with excellent electrical properties of Cu-Cu bonding has been revealed. Furthermore, filling the molding compound into the gaps between Cu joints to prevent further oxidation has become a great challenge. Currently, metal/dielectric hybrid bonding could be one of the best solutions to fabricated ultra-high-density I/O devices with excellent bonding strength and electrical properties. However, defects (voids) in the bonding interface are unavoidable due to the atomic diffusion in metals. It has been reported that the electrical resistance of devices is highly related to interfacial voids. Thus, interfacial analyzing tools for void observation at the bonding interface are crucial. In this study, we demonstrate a continuous etching quasi-in situ observation using a focused ion beam (FIB), scanning electron microscope (SEM), and electron backscattered diffraction (EBSD). Results show reliable data of void quantization and variation in size and distribution at the bonding interface.

Conclusion

Cut-&-view FIB and EBSD have been successful performed in fine-pitch Cu/SiO_2 hybrid joints. Voids that formed at the bonding interface can be effectively quantized in a bigger observation area.

The crystal orientation of the whole Cu joint can be observed and thus the particular orientation ratio and grain size distribution can be obtained.

METHODS

The target structure was etched using FIB parallel for the interfacial void observation and perpendicular to the bonding interface for the crystal orientation observation. The etching direction illustrated in Figure 1.

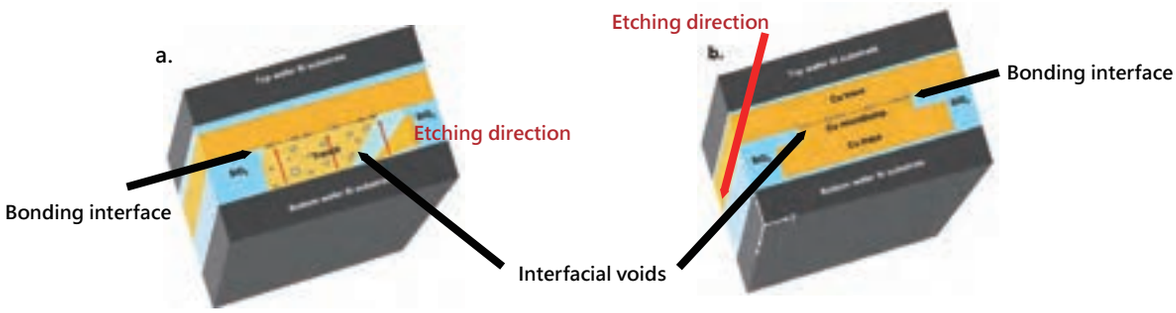

FIGURE 1. SCHEMATICS OF CUT & VIEW TECHNIQUES FOR (A)INTERFACIAL VOIDS AND (B)CRYSTAL ORIENTATION OBSERVATION.

RESULTS

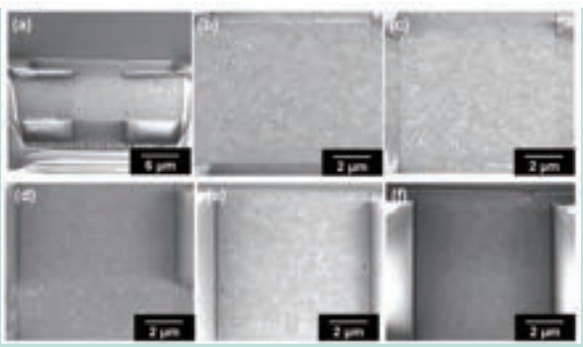

FIGURE 2. ELECTRON IMAGES OF (A)OVERVIEW STRUCTURE, (B)NEARBY, (C)AT, AND (D)BEYOND THE BONDING INTERFACE. CU TRACE APPEARED AFTER ETCHING FOUND IN (E)AND (F).

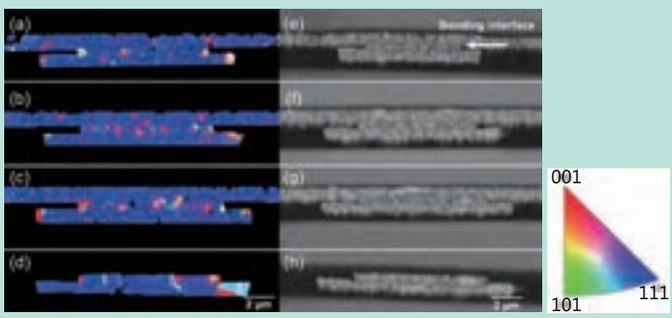

FIGURE 3 (A~D)THE INVERSED POLE FIGURE OF THE WHOLE JOINT STRUCTURE AND (E~F)CORRESPONDING MICROSTRUCTURE OBSERVATION AT THE SAME PLACE.

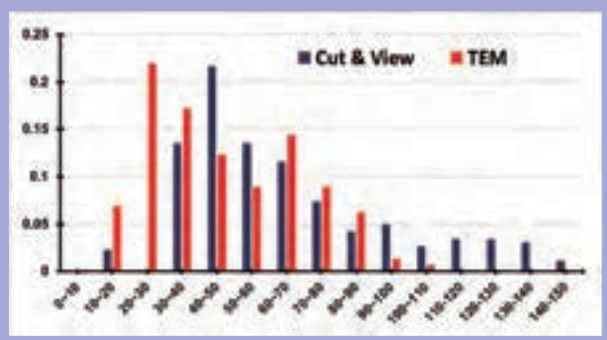

FIGURE 4 INTERFACIAL VOIDS ANALYSIS COMPARISONS WITH CUT & VIEW TECHNIQUES AND TEM.

Discussions

Figure 2(a) shows the overview of the etched structure using the Cut and View technique for voids distribution calculation. The images captured nearby, at, and beyond the bonding interface are shown in Figure 2(b), (c) and (d) while the Cu trace appeared after etching found in Figure 2(e), (f). The voids at the bonding interface can be clearly observed and further calculated the distribution and the total area of the voids by using image J. We compare the results with the TEM analysis and found that by using Cut & view techniques, it is relatively lower cost and time-consuming during sample preparation. Furthermore, a larger observation area can also be provided compared to TEM analysis. Unlike TEM, voids at 0~10 nm in diameter are hardly observed by cut & view technique. However, it is more sensitive to the bigger voids with a diameter of 90~150 nm which TEM couldn't which shown in Figure 4.

Furthermore, cross-sectional cut and view EBSD analysis was carried out and thus we are able to observe the crystal orientation for almost the whole structure in a cross-sectional direction. Figure 3(a~d) illustrates the inversed pole figure of the whole joint structure while Figure 3(e~h) shows the corresponding microstructure observation at the same place. As the value was calculated by using OIM (orientation imaging microscopy), we found the average grain size is around ~400 nm and the (111) ratio reached 80%. Therefore, this could further explain the contribution of the Cu with highly 111 oriented in low-temperature bonding.

National Yang Ming Chiao Tung University
Chao, Tien-sheng

Fabrication of Bilayer Stacked Antiferroelectric/Ferroelectric $Hf_xZr_{1-x}O_2$ FeRAM and FeFET with Improved Leakage Current and Robust Reliability by Modifying Atomic Layer Deposition Temperatures

通過調變原子層沉積溫度製造雙層堆疊反鐵電/鐵電電晶體以改善漏電流與增強可靠度測試

Tien-sheng Chao 趙天生

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-016.

*This study also received supports from NSTC, and TSRI.

Introduction

Ferroelectric (FE) materials with hafnium-based have attracted attention in recent years owing to their complementary metal—oxide—semiconductor compatibility. Applications of ferroelectric materials have been reported in many studies, such as ferroelectric random-access memory (FeRAM), ferroelectric field effect transistor (FeFET), negative capacitance field effect transistor (NCFET), and ferroelectric tunnel junction memory (FTJ).

The leakage current is a critical issue for reliability tests. In particular, the leakage current can be inhibited by inserting an Al_2O_3 dielectric layer into a HZO layer, doping Al into HfO_2 (HfAlO: HAO), or doping Al into HZO. However, the remnant polarization (Pr) value is also affected, which means that the memory window (MW) is difficult to use in nonvolatile memory (NVM) devices.

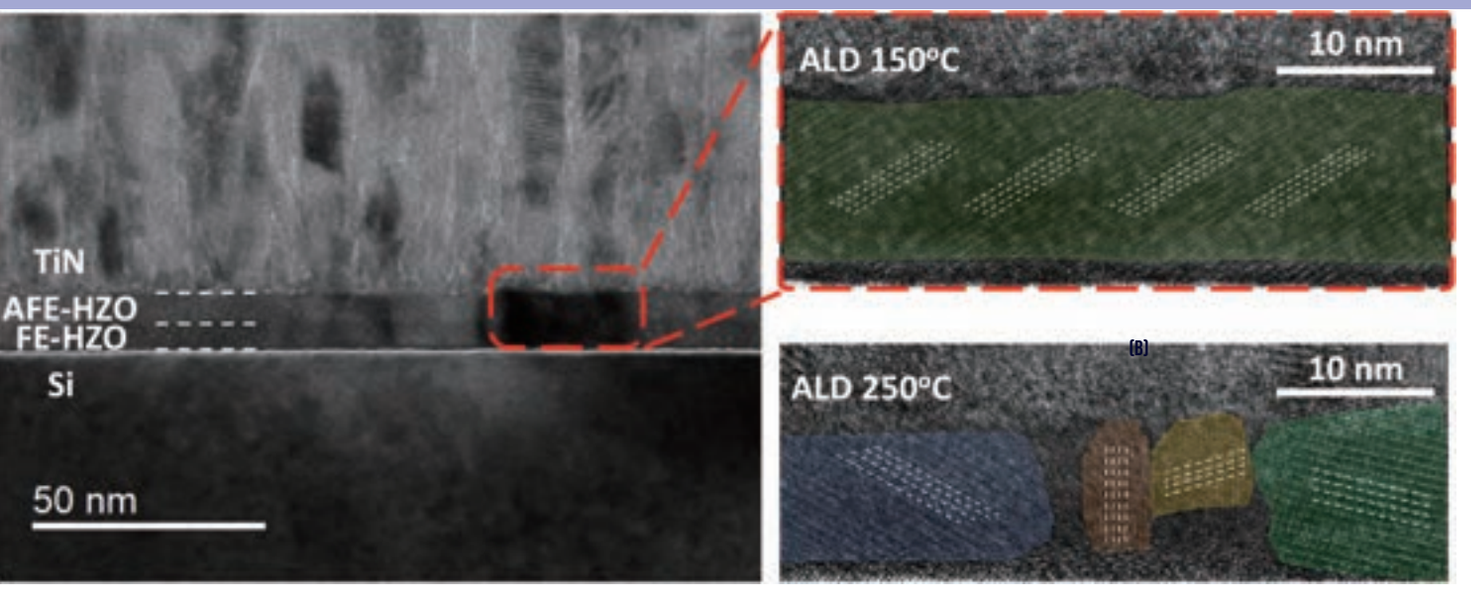
In this research, we stacked bilayer HZO to enhance the reliability tests and control the grain size by modifying the atomic layer deposition (ALD) temperature to reduce the leakage current. The results of transfer characteristic (I_d—V_g) curves and endurance test between different ALD temperatures were compared. The proposed approach is a candidate for the next generation of NVM applications.

Conclusion

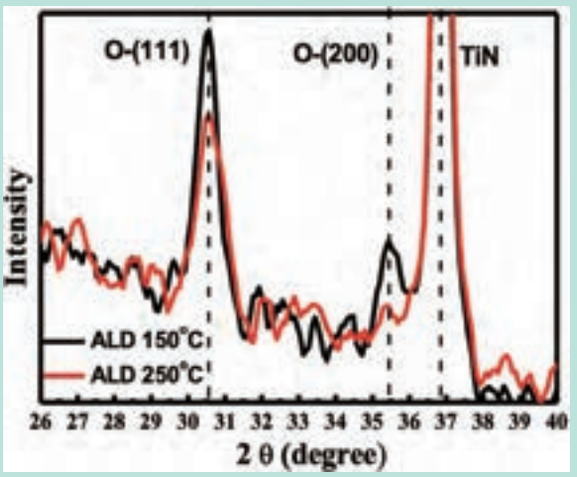
FeFET of bilayer HZO with low leakage current and robust reliability tests were fabricated by modifying an ALD temperature. TEM results showed that the AFE and FE layers were separated. Large MW (> 1.5V), high gate control ability, and robust endurance (> 10^7 cycles) were observed at a low ALD temperature. These properties suggest that a low ALD temperature approach is a promising process for use in NVMs.

MATERIALS ANALYSIS

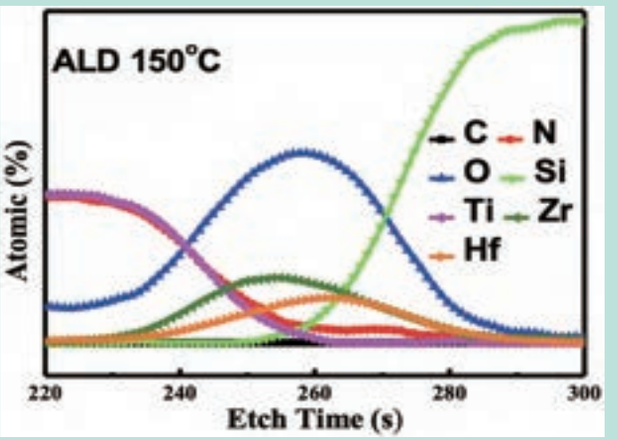
Fig. 1. (A) The cross-section HR-TEM of bilayer HZO. The AFE-HZO and FE-HZO are separated. (B) and (C) show the zoom-in image for ALD 150˚ C and 250˚ C, respectively. ALD 150˚ C devices exhibit large grain and less grain boundary. (D) The XPS results for the FeFET with ALD 150˚ C devices. (e) The GI-XRD results of ALD 150˚ C and 250˚ C.



(A) (B) (C)



(D)



(E)

Results & Discussion

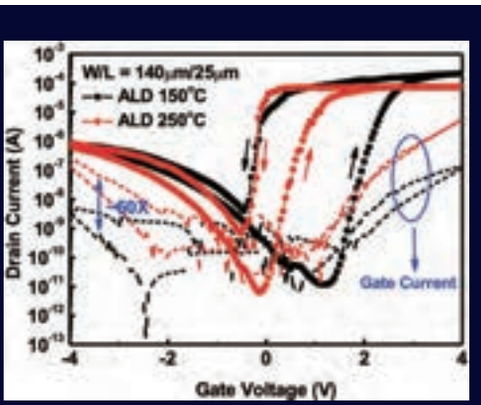


Fig. 2. The I_d–V_g curves of the bilayer HZO for ALD 150°C and 250°C. The ALD 150°C devices exhibit a large MW and a low gate current.

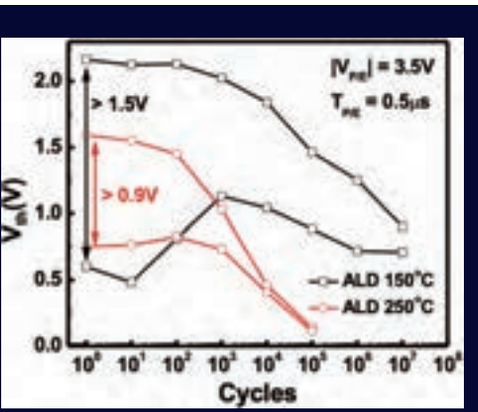


Fig. 3. The endurance with FeFET for ALD 150°C, and 250°C devices. More than 107 cycles exhibited in ALD 150°C devices.

National Yang Ming Chiao Tung University

Li, Pei-wen

GERMANIUM QUANTUM-DOT SINGLE-HOLE TRANSISTORS WITH SELF-ORGANIZED TUNNEL BARRIERS AND SELF-ALIGNED ELECTRODES

可高溫運作之鍺量子點單電洞電晶體

Pei-wen Li 李佩雯

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賴祈正/邱鈺雯/張佑銘

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-017.

*This study also received supports from TSRI.

Introduction

We report the fabrication and electrical characterization of single-hole transistors (SHTs), in which a Ge spherical quantum dot (QD) weakly couples to self-aligned electrodes via self-organized tunnel barriers of Si_3N_4. A combination of lithographic patterning, sidewall spacers, and self-assembled growth was used for fabrication. The core experimental approach is based on the selective oxidation of poly-SiGe spacer islands located at the specially designed included-angle locations of Si_3N_4/Si-trenches. By adjusting processing times for conformal deposition, etch back and thermal oxidation, good tunability in the Ge QD size and its tunnel-barrier widths were controllably achieved.

Each Ge QD is electrically addressable via self-aligned Si gate and reservoirs, thus offering an effective building block for implementing single-charge devices. Tunneling current of the Ge-QD SHTs was measured at T = 4 - 40 K, featuring aperiodic oscillatory current and negative differential conductance behaviors. Estimated single-hole addition energies for N = 0 → 1 and 1 → 2 are 145 meV and 49 meV, respectively

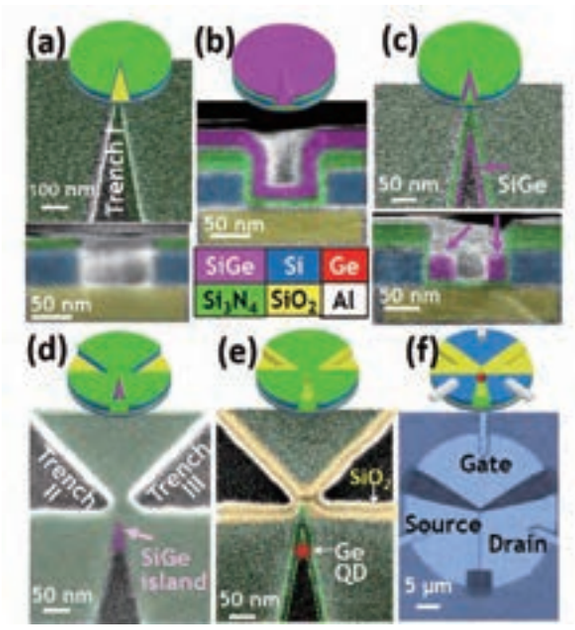
Conclusion

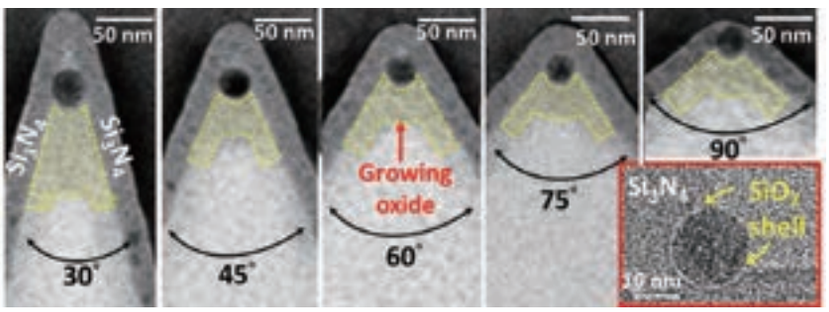
We have advanced the state-of-the-art for the fabrication of Ge-QD SHTs with self-organized tunnel barriers and self-aligned electrodes using an ingenious combination of lithographic patterning, sidewall-spacer technique, and self-assembled growth. The self-aligned electrodes do indeed suppress the gate overlap of the S/D electrodes thereby improving the Coulomb oscillatory current with higher PVCRs. Our Ge QD SHTs feature aperiodic oscillatory current and NDC behaviors within the temperature range of 4 – 40 K with corresponding estimated addition energies > 49 meV for few holes regime.

Thanks to large addition energies and well-separated energy levels, our small Ge QDs with few-charges are desirable for many applications including metrology, electrometry, and quantum registers from technological perspectives.

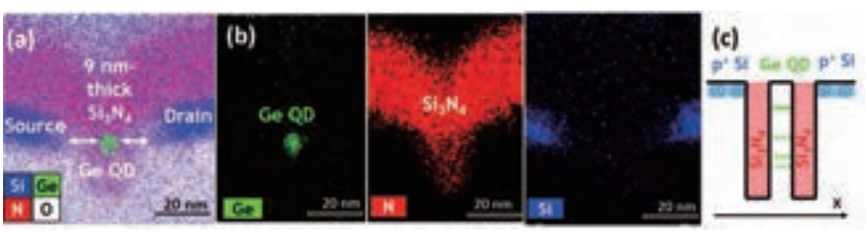
EXPERIMENTAL FABRICATION OF Ge QDS SHTS

Precision fabrication of Ge-QDs at designated included-angle locations

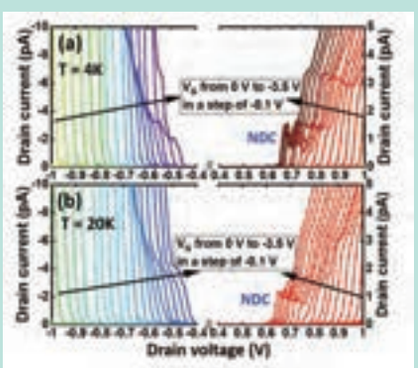


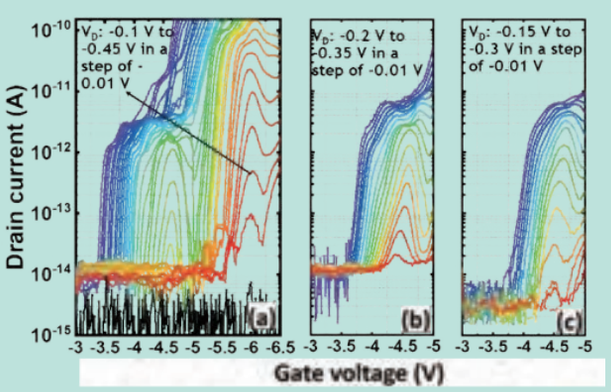


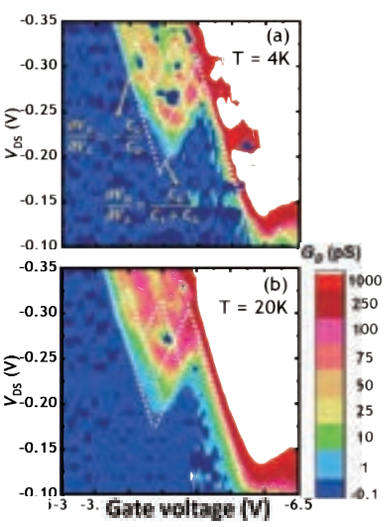
Self-aligned source/drain



RESULTS







Discussion

We have advanced the state-of-the-art for the fabrication of Ge-QD SHTs with self-organized tunnel barriers and self-aligned electrodes using an ingenious combination of lithographic patterning, sidewall-spacer technique, and self-assembled growth.

The self-aligned electrodes do indeed suppress the gate overlap of the S/D electrodes thereby improving the Coulomb oscillatory current with higher PVCRs. Our Ge QD SHTs feature aperiodic oscillatory current and NDC behaviors within the temperature range of 4 – 40 K with corresponding estimated addition energies > 49 meV for few holes regime.

Thanks to large addition energies and well-separated energy levels, our small Ge QDs with few-charges are desirable for many applications including metrology, electrometry, and quantum registers from technological perspectives.

National Yang Ming Chiao Tung University

Horng, Ray-hua

STUDY ON PROPERTIES OF SI IN-SITU DOPING HETEROEPITAXY β-GA203 BY MOCVD

利用有機金屬化學氣相沉積系統成長摻雜氧化鎵異質磊晶膜之研究

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This study is supported by Materials Analysis Technology Inc. under contract 2022-T-018.

Introduction

Recently, ß-Ga_2O_3 has attracted significant interest due to its potential for high power devices, which can be attributed to its material characteristics, such as a wider band gap and a high critical electric field. Ga_2O_3′ s Barliga figure of merit (BFOM) value is 3444, which is ten times that of SiC and four times of that of GaN [However, the resistance of intrinsic Ga_2O_3 material is almost insulating (>10^{14} Ω), which limits its real applications in industry.

In this study, a tetraethoxysilane (TEOS) precursor was used as the Si source for in-situ doping Ga_2O_3 epilayer, which is a low-cost and safer alternative to traditional Silane (SiH_4) source which is highly explosive and requires costly facility construction. Moreover, TEOS exhibits excellent uniformity during Ga_2O_3 epitaxial growth on heterogeneous sapphire substrates using metalorganic chemical vapor deposition (MOCVD). The detailed electrical properties and surface morphologies of Ga_2O_3 epilayers with various TEOS mole flow rate were investigated.

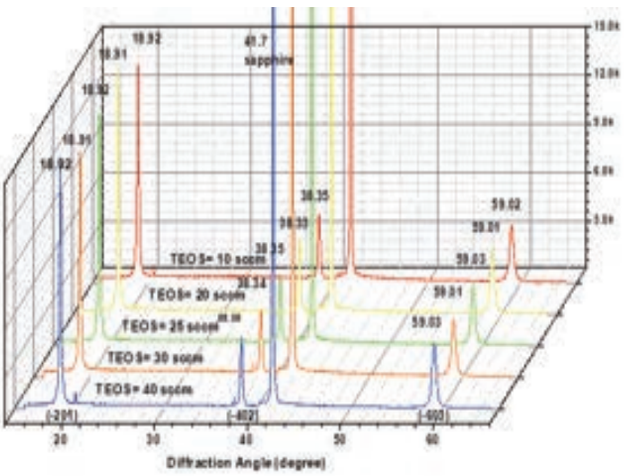
Conclusion

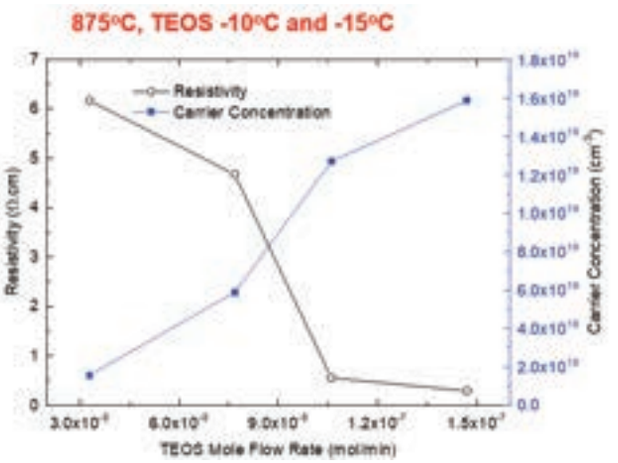
- High quality Ga_2O_3 epilayer with Si *in-situ* doping grow by MOCVD.
- By XRD data, the as-deposited Ga_2O_3 epilayer was β-phase and the Ga_2O_3 epilayer still kept pure β-phase for the TEOS molar flow vary from 2.23×10^{-7} to 6.67×10^{-7} mol/min.
- High Si doping concentration can be achieved by MOCVD *in-situ* doped, according to SEMI's examine.
- It revealed Si doping concentrations of 5.5×10^{19} atom/cm^3, 1.1×10^{20} atom/cm^3, and 1.4×10^{20} atom/cm^3 for TEOS flows of 2.23×10^{-7}, 4.47×10^{-7} to 6.67×10^{-7} mol/min.

RESULTS & DISCUSSION

By the XRD, there are no obviously different between the TEOS flow from 10 sccm to 40 sccm, the crystalline was very similar between them

As the TEOS flow rate increased, the sheet resistance reduced and the carrier concentration increasing. It indicated that the TEOS contributes the Si to replaced the Ga position which effectively donate the electrons and improve the conductivity

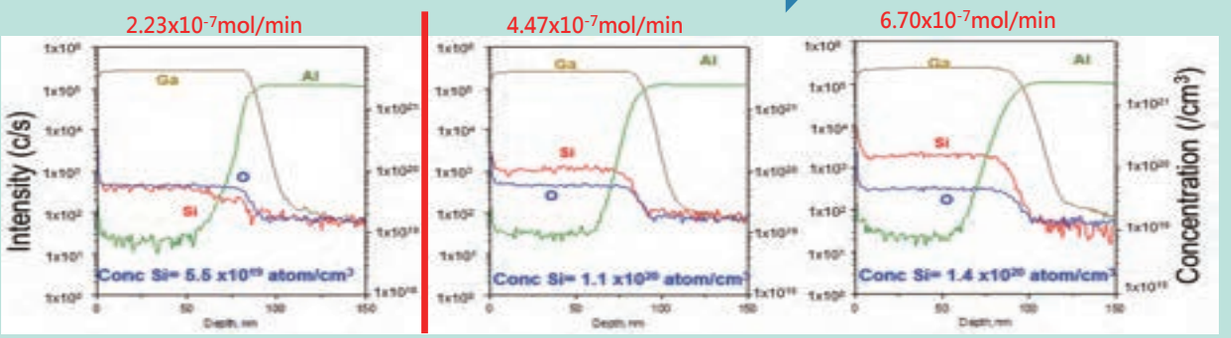




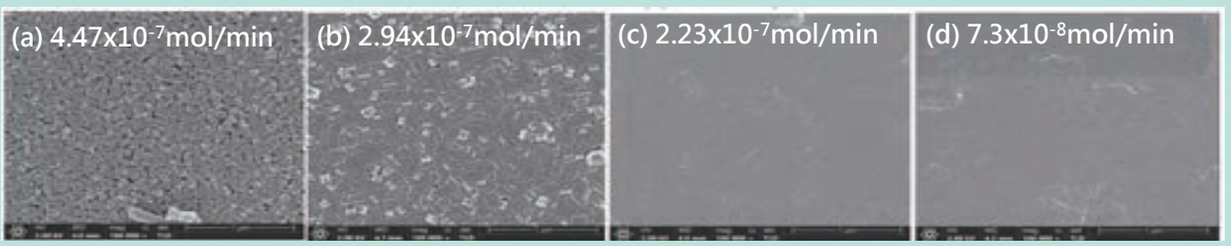
MOCVD growth temp = 825 ^{0}C

Saturations

CORRESPONDING CONCENTRATION WAS 5.5 X10^{19}/CM^3, 1.1 X10^{20}/CM^3 AND 1.4X10^{20}/CM^3 FOR THE Ga_2O_3 DOPED BY TEOS MOLE RATE BEING 2.23X10^{-7}, 4.47X10^{-7} AND 6.70X10^{-7} MOLE/MIN, RESPECTIVELY.



BUT THE DOPANT MOLE RATE OF TEOS WAS 2.94X10^{-7} MOLE/MIN AND 4.47X10^{-7} MOLE/MIN, THE MORPHOLOGIES CHANGED A LOT AND PRESENTED SMALL RECTANGULAR ON THE SURFACE.



Material & Methods

The high-quality β-Ga_2O_3 epilayers were grown on c-plane (0001) sapphire substrates using metalorganic chemical vapor deposition (MOCVD) with trimethylgallium (TEGa) and oxygen (O_2) as precursors for Ga and O, respectively. In-situ doping during Ga_2O_3 epilayers growth was achieved using TEOS as the Si doping source. High-purity Ar was used as the carrier gas for TEGa and TEOS, and N_2 was used as the main flow of MOCVD. The growth pressure and temperature were 25 Torr and 825°C-875°C, respectively.

The crystal structure and orientation were determined by X-ray diffraction system. The surface morphology and thickness of the β-Ga_2O_3 epilayers were observed by scanning electron microscopy (SEM). Si in-situ doping concertation was analyzed by SIMS. The electrical conductivities were evaluated using current-voltage measurement with a four-point probe station or semiconductor parameter analysis instrument. The surface roughness of β-Ga_2O_3 epilayers was measured using an atomic force microscope (AFM, Dimension 5000).

National Yang Ming Chiao Tung University

Tsui, Bing-yue

A STUDY OF OHMIC CONTACT TECHNOLOGY OF SMALL-AREA METAL/P+ SILICON CARBIDE

小面積金屬/P+碳化矽歐姆接觸技術研究

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王家陽(Chia-yang Wang)

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-019.

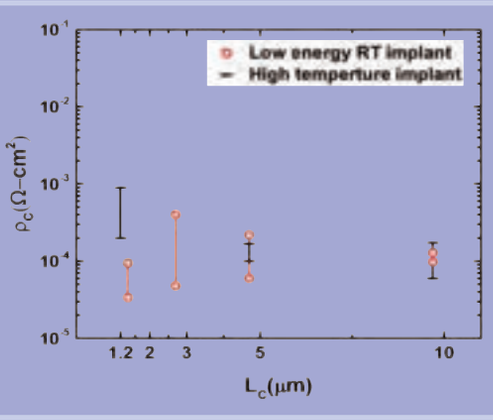
Introduction

- SiC is known as a promising material for high-power devices because of wide bandgap, high critical electric field, and high thermal conductivity.
- Contact resistivity (ρ_c) is always an essential part in device optimization because reducing the ρc can increase the turn-on current and reduce power loss.
- Achieving ohmic contact on p-type SiC is difficult because of the high Schottky barrier height and its low ionization rate.
- It has been reported that the contact becomes non-ohmic as the contact window becomes smaller than 20 μm.
- In this project, we optimized the processing conditions for achieving ohmic contact between TiAl and p-type SiC and obtained a record-low ρ_c value of 3×10^{-5} Ω-cm^2 at record-small contact area of 1.5 μm × 1.5 μm through defect engineering.

Conclusion

The area dependence of the contact resistance on p-type SiC using TiAl-based metal can be solved by damaging the SiC surface prior to metal deposition, which results in lowering of ρ_c . Moreover, The defects produced during LERT ion implantation may promote trap-assisted tunneling. In this study, a record-low contact resistivity of 3×10^{-5} Ω cm^2 was achieved for p-type SiC with TiAl in a record-small contact area of 1.5 μm.× 1.5 μm. Additionally, interface uniformity should be improved by future studies to reduce the contact resistance.

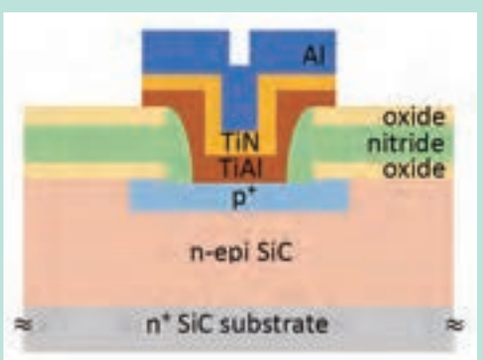
RESULTS



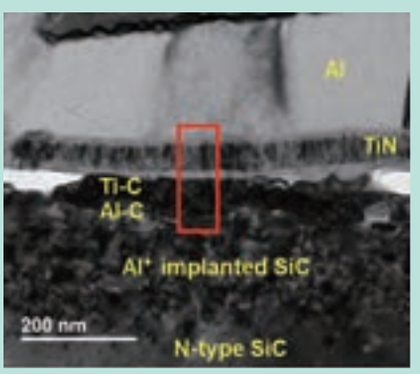
- Metal contact on p-type SiC with a record-low specific contact resistance of 3 × 10−5 Ω-cm² at record-small contact area of 1.5 μm × 1.5 μm was obtained in this study.
- This results has been published in the IEEE Electron Device Letters.

B. Y. TSUI, Y. L. CHEN, AND S. H. LAI, "METAL CONTACT ON P-TYPE 4H-SIC WITH LOW SPECIFIC CONTACT RESISTANCE AND MICROMETER-SCALE CONTACT AREA," IEEE ELECTRON DEVICE LETT., VOL.44, NO.9, PP. 1539-1542, 2023. DOI: 10.1109/LED.2023.3299688.

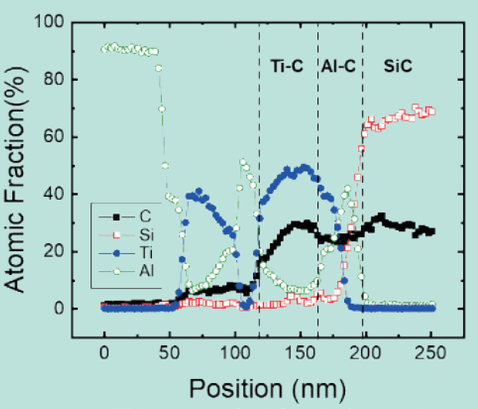
MATERIALS & METHODS



- Cross-Bridge Kelvin Resistor (CBKR) was used to extract accurate ρ_c.



- Cross-sectional TEM was used to inspect the contact structure.



- EDX was used to identify the interface atomic composition.

Discussion

- Ar plasma treatment enhances Al-Si-C layer formation
- LERT process promotes trap-assisted tunneling
- High temperature (HT) implantation forms low resistance P^+ layer and low leakage current junction.

National Taiwan University

Liu, Chee-wee

MATERIAL CHARACTERIZATION OF STACKED GeSi/GeSn NANOSHEETS/ULTRATHIN BODIES, TREEFETS, C(COMPLEMENTARY)FETS AND EXTREMELY LOW S/D RESISTIVITY/CONTACT RESISTIVITY

鍺矽/鍺錫垂直堆疊通道電晶體,極薄通道,樹狀電晶體,互補式電晶體與超低源極/汲極接觸電阻之材料特性分析

Chee-wee Liu 劉致為

Department of electrical engineering,
National Taiwan University, Taiwan

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Research Team:

Wan-hsuan Hsieh (謝宛軒) Wei-jen Chen (陳韋任)

This study is supported by Materials Analysis Technology Inc. under contract 2022-T-020.

Introduction

Device Roadmap for More Moore Scaling
後摩爾時代之元件技術路線圖

- THE STACKED GAAFET IS EXPECTED TO REPLACE FINFET FOR BETTER PERFORMANCE-POWER-AREA (PPA).
- GE-BASED MATERIAL FOR HIGH MOBILITY CHANNEL (HMC).

2023 VLSI Taiwan Paper Count
(technology + Joint Focus Session)

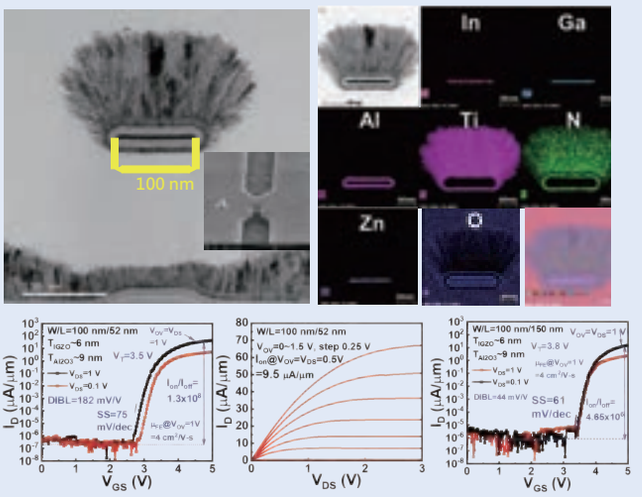
Affiliation	Session (The survey is based on the affiliation of the first author)	Total number
TSMC	T1-4, T8-1, T13-3, T15-3, T16-1, JFS4-2(invited)	6
National Taiwan Univ (劉致為)	T5-3, T12-4, T16-4, T17-3, T10-2(第一作者affiliation同時屬台大與師大，為劉致為教授學生, 與李敏鴻教授合作),	5
National Yang Ming Chiao Tung Univ	T14-2, T18-5, T2-4 (第一作者affiliation同時屬陽交大與師大)	3
National Taiwan Normal Univ	T2-4, T10-2	2
National Tsing Hua Univ	T9-4	1
Industrial Technology Research Institute of Taiwan, Taiwan	T18-5	1

MATERIAL ANALYSIS TECHNOLOGY INC.

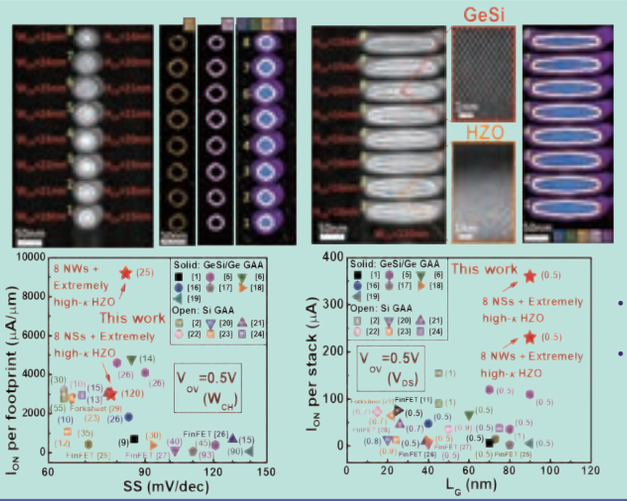
A-IGZO GAA NANOSHEET FET
非晶態氧化銦鎵鋅閘極環繞式奈米片電晶體

(J.-C. CHIU ET AL. AND C. W. LIU, 2023 VLSI)

- First demonstration of a-IGZO GAA nanosheet FETs by channel release and ALD gate stack.
- BEOL compatible process temperature of ≤ 300 °C.
- Achievable small SS=61mV/dec, I_{off} <10^{-7} mA/mm, I_{on}/I_{off}>1.3x10^8 and positive V_T=3.5 V.
- Scaled channel length of 52 nm.

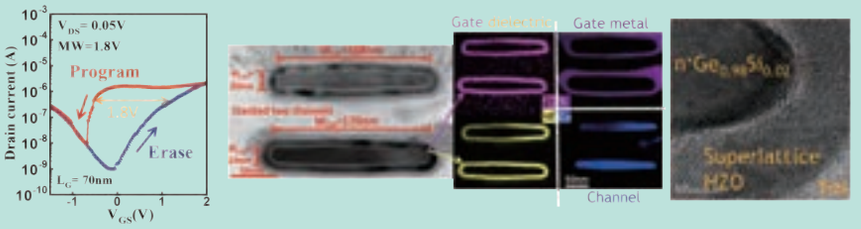


RESULT & CONCLUSION



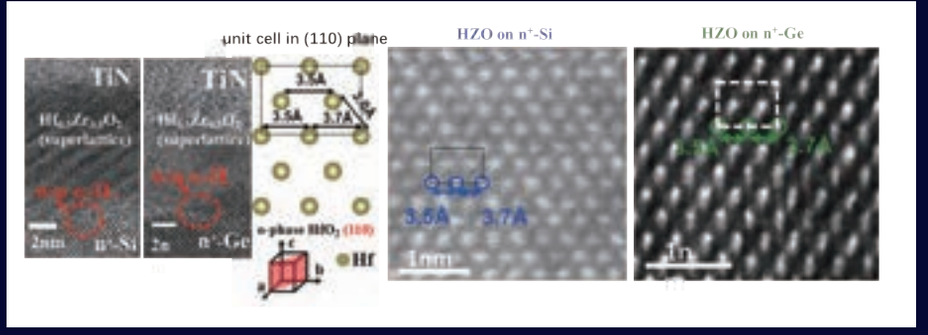
8 STACKED $Ge_{0.95}Si_{0.05}$ NANOWIRES AND NANOSHEETS WITH HIGH-κ $Hf_{0.2}Zr_{0.8}O_2$
八層垂直堆疊鍺矽奈米線通道搭配高介電常數二氧化鉿/鋯介電層
(Y.-C. LIU ET AL. AND C. W. LIU, 2023 VLSI)

- The extremely high-High-κ $Hf_{0.2}Zr_{0.8}O_2$ gate stacks are integrated into both the 8 stacked $Ge_{0.95}Si_{0.05}$ nanowires and nanosheets.
- Record ION per footprint of 9200μA/μm (nanowires) and the record ION per stack of 360μA (nanosheets) at V_{OV}=V_{DS}=0.5V, respectively, among reported Si/GeSi/Ge 3D nFETs.



2 STACKED $Ge_{0.95}Si_{0.05}$ NANOSHEET N-FEFET
二層垂直堆疊鍺矽奈米線通道鐵電電晶體
(Y.-C. LIU ET AL. AND C. W. LIU, 2023 VLSI)

- Superlattice FE HZO is integrated into stacked NS FeFET with the high MW of 1.8V at low write voltage.
- The $Ge_{0.98}Si_{0.02}$ NSs are surrounded by FE HZO superlattice and in-situ TiN to ensure the GAA structure.
- No amorphous IL formation between GeSi channel and superlattice FE layer is confirmed by HR-TEM.



Towards Epitaxial Ferroelectric HZO on n+-Si/Ge Substrates
磊晶成長鐵電二氧化鉿鋯於矽鍺基板

(Z.-F. Zhao et al. and C. W. Liu, 2023 VLSI)

- The a-IL free is possible for Si and Ge if correct HF dipping.
- According to the symmetric lattice, the c-axis of o-phase is well-aligned along growth direction as compared to simulation.

Contact

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MATERIAL ANALYSIS TECHNOLOGY INC.
Industry-Academia Cooperation 2022